INDEX

AIM OF THE EXPERIMENT:

Introduction to digital electronics.

DEFINATION OF DIGITAL ELECTRONICS:

i) Digital electronics is a branch of electronics that deals with two digits i.e. 0 & 1.Here, 0 means low logic or false and 1 means high logic or true.
ii) Digital electronics involving study about the digital signal use and produce them.
iii) Digital electronics operates to including different types of gates and that gates are binding with integral circuit.

REQUIREMENTS TO CONDUCT DIGITAL ELECTRONICS LAB:

a) Digital electronics trainer kit.
b) Power connection.
c) Connector
d) Gloves

ADVANTAGES OF DIGITAL ELECTRONICS:

a) Digital systems are easier to design.
b) Information storage is easy.
c) Accuracy is very high.
d) Digital circuits are less affected by noise.
e) Easy to perform error detection and execution with digital signal.
f) Integrated circuits are mostly used in the digital electronics, so that size of digital devices are small.

DISADVANTAGES OF DIGITAL ELECTRONICS:

i) Heat will be more when digital circuits are working more time.
ii) Digital circuits require a power supply. iii) Digital circuits consume more energy or power as compare to any circuits.
iv) More complex circuits.
v) When one IC will be damaged it must affect to others.

APPLICATION OF DIGITAL ELECTRONICS:

i) Digital watch ii) Refrigerator iii) Speedometer iv) Traffic light
v) Automatic glass door in offices and restaurant.
vi) Rocket science.
vii) ATM card viii) Computer & laptops.

CONCLUSION:

We concluded that the above experiment has been done by me successfully.

AIM OF THE EXPERIMENT:

To study about NOT gate.

APPARATAUS REQUIRED:

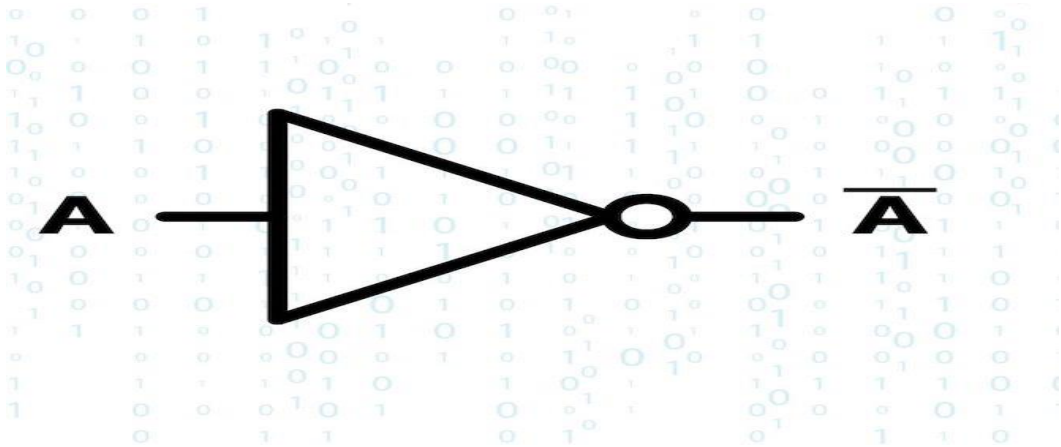
i) Digital electronics kit ii) Probes(connectors) iii) Power supply TRUTH TABLE:

INPUT	OUTPUT
A	$\overline{A}$
0	1
1	0

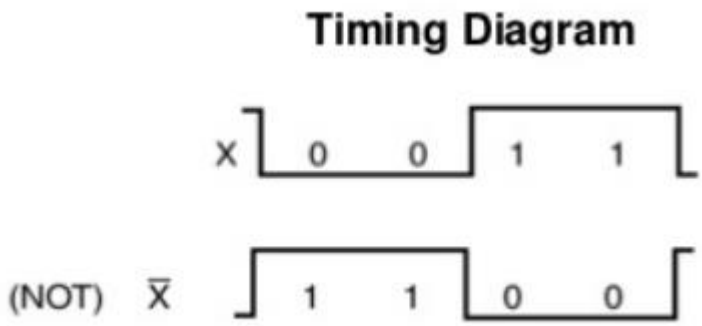
CONCLUSION:

We concluded that the above experiment has been done by me successfully.

GATE DIAGRAM:-



TIMING DIAGRAM:-



AIM OF THE EXPERIMENT:-

To study about OR gate

APPARATUS REQUIRED:-

i. Digital trainer kit. ii. Probes (connector)
iii. Power Supply.

TRUTH TABLE:-

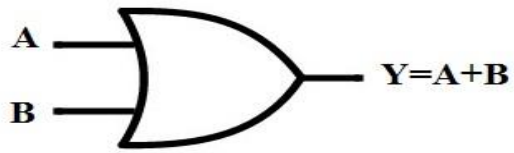
Input		Output
A	B	Q=A+B
0	0	0
0	1	1
1	0	1
1	1	1

.

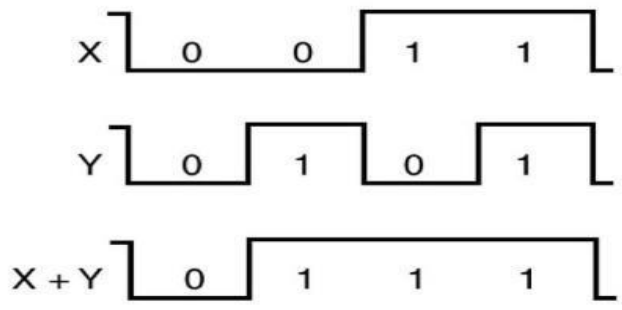
CONCLUSION:-

We concluded that the above experiment has been done successfully by us.

LOGIC GATE DIAGRAM:-



TIMING DIAGRAM:-



AIM OF THE EXPERIMENT:- To

study about AND gate.

APPARATUS REQUIRED:-

i. Digital trainer kit
ii. Probes(connectors)
iii. Power supply

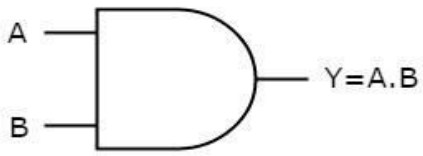
TRUTH TABLE:-

Input		Output
A	B	Q=A.B
0	0	0
0	1	0
1	0	0
1	1	1

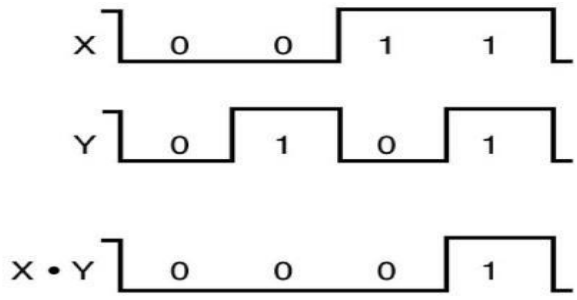
CONCLUSION:-

We concluded that the above experiment has been done by us successfully.

AND GATE DIAGRAM:-



TIMING DIAGRAM:-



AIM OF THE EXPERIMNT:- To

study about NAND logic gate

APPARATUS REQUIRED:-

i. Digital trainer kit
ii. Probes(connection)
iii. Power supply

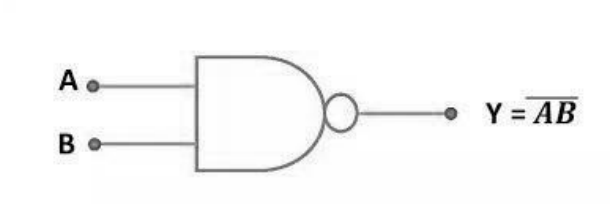
TRUTH TABLE:-

INPUT		OUTPUT
A	B	$Q=\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

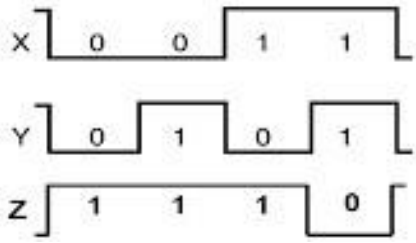
CONCLUSION:-

We concluded that the above experiment has been done by us successfully. NAND gate

diagram:-



Timing diagram:-



Aim of the experiment:-

To study about NOR logic gate Apparatus

Required:-

i)Digital trainer kit ii)

probes (connector) iii)

Power supply

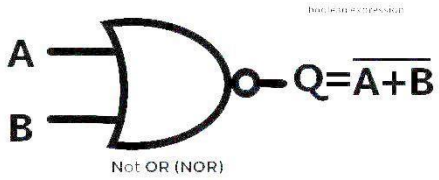
Truth Table:-

INPUT		OUTPUT
A	B	$Q=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

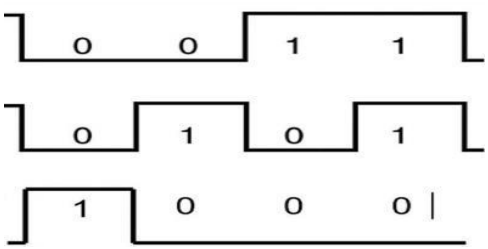
:-

Conclusion:- We conclude that the above experiment has been done by successfully

Logic gate diagram :-



Timing diagram:-



EXPERIMENT-7

Aim of the Experiment-

To study about x-or gate

Apparatus Required:-

i)Digital trainer kit. ii)probes(connector).

iii)power supply.

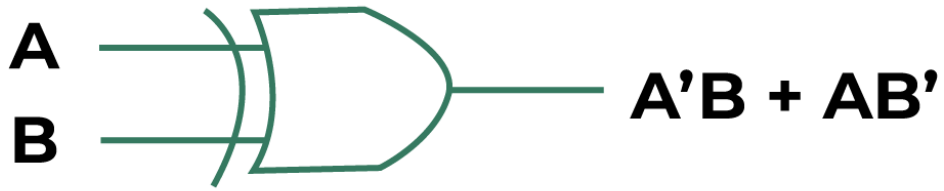
Truth Table:-

INPUT		OUTPUT
A	B	$Q=A\bar{B}+\bar{A}B$
0	0	1
0	1	0
1	0	0
1	1	1

Conclusion:-

We concluded that the above experiment has been done by us successfully.

GATE DIAGRAM:-



Aim of the Experiment-

To study about x-nor gate

Apparatus Required:-

i)Digital trainer kit. ii)probes(connector).

iii)power supply.

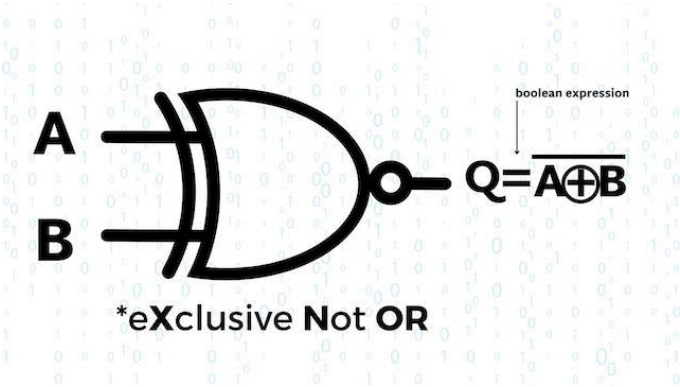
Truth Table:-

INPUT		OUTPUT
A	B	Q=AB+AB
0	0	1
0	1	0
1	0	0
1	1	1

Conclusion:-

We concluded that the above experiment has been done by us successfully.

GATE DIAGRAM:-



AIM OF THE EXPERIMENT:-

To implement various gates by using universal properties of NAND gates, verify and truth table tabulate data.

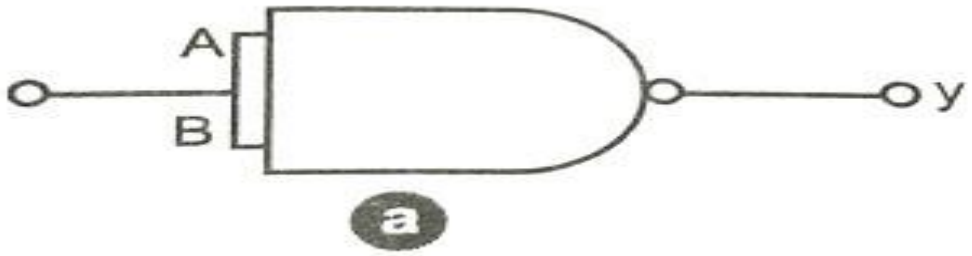
APPARATAUS REQUIRED:-

i) Digital electronic kit ii) Probes(connector) iii) Power supply

TRUTH TABLE:-

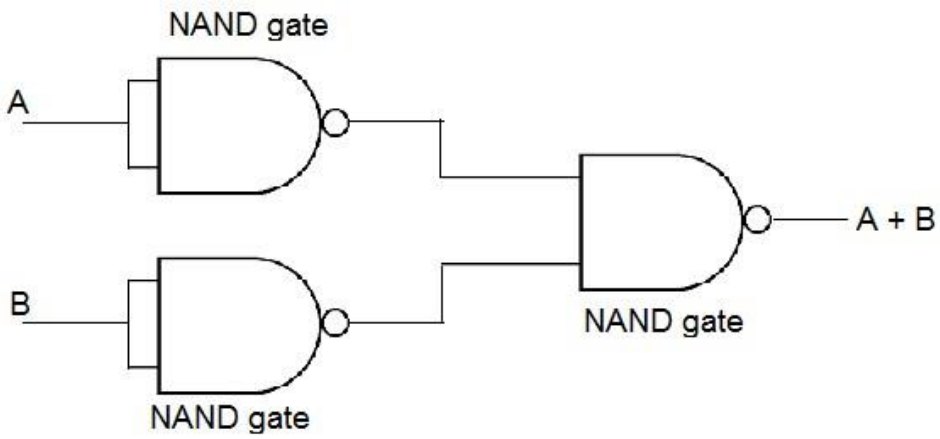
i) NOT gate using NAND gate

Input	Output
A	Y
0	1
1	0



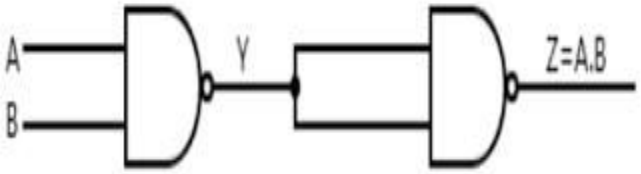
ii) OR gate using NAND gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



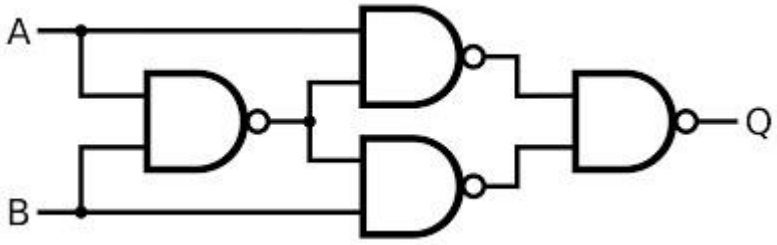
iii) AND gate using NAND gate

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



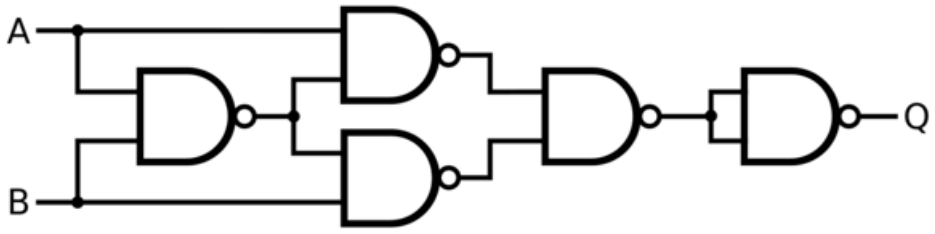
iv) X-OR gate using NAND gate

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0



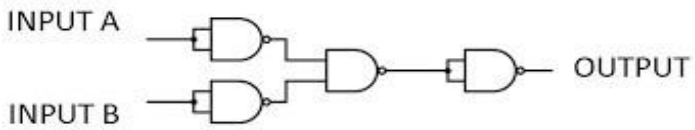
v) X-NOR gate using NAND gate

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1



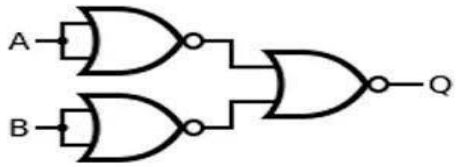
NOR gate using NAND gate:-

INPUT		OUTPUT
A	B	$\overline{Q=A.B}$
0	0	1
0	1	0
1	0	0
1	1	0



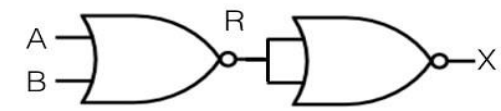
AND gate using NOR gate:-

Input		Output
A	B	Q=A.B
0	0	0
0	1	0
1	0	0
1	1	1



OR gate using NOR gate:-

Input		Output
A	B	Q=A+B
0	0	0
0	1	1
1	0	1
1	1	1



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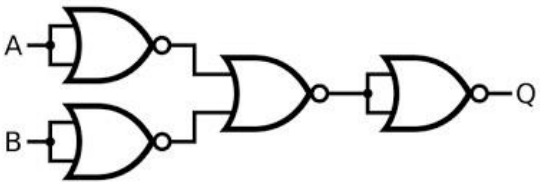
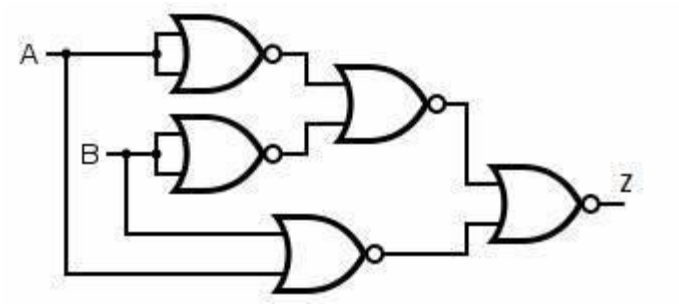
NAND gate using NOR gate:-

INPUT		OUTPUT
A	B	$\overline{Q=A.B}$
0	0	1
0	1	1
1	0	1
1	1	0



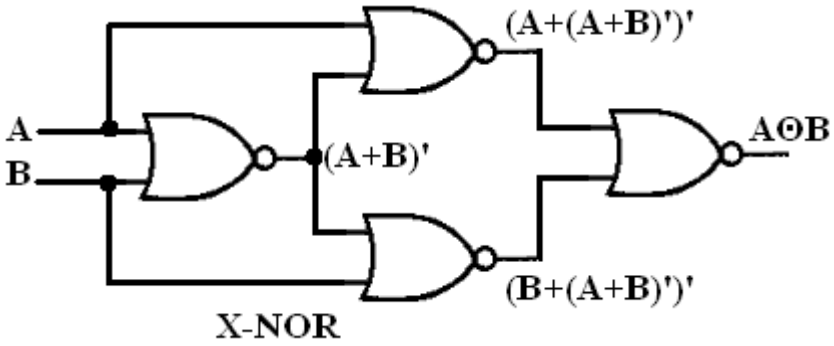
XOR gate using NOR gate:-

INPUTS		OUTPUTS
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



X-NOR gate using NOR gate:-

A	B	A **XNOR** B
0	0	1
0	1	0
1	0	0
1	1	1



AIM OF THE EXPERIMENT

To construct and verify operation of half adder & full adder using logic gates.

APPARATUS REQUIRED

i. Digital trainer Rit. **ii.** Probes (Connector)

iii. Power supply.

TRUTH TABLE

Half adder

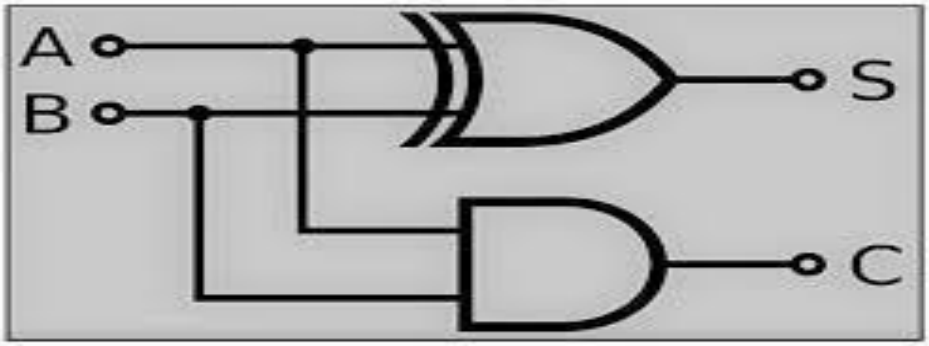
Input		Output	
A	B	Sum(s)	Carry(c)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder

Input			Output	
A	B	C	Sum(s)	Carry(c)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1

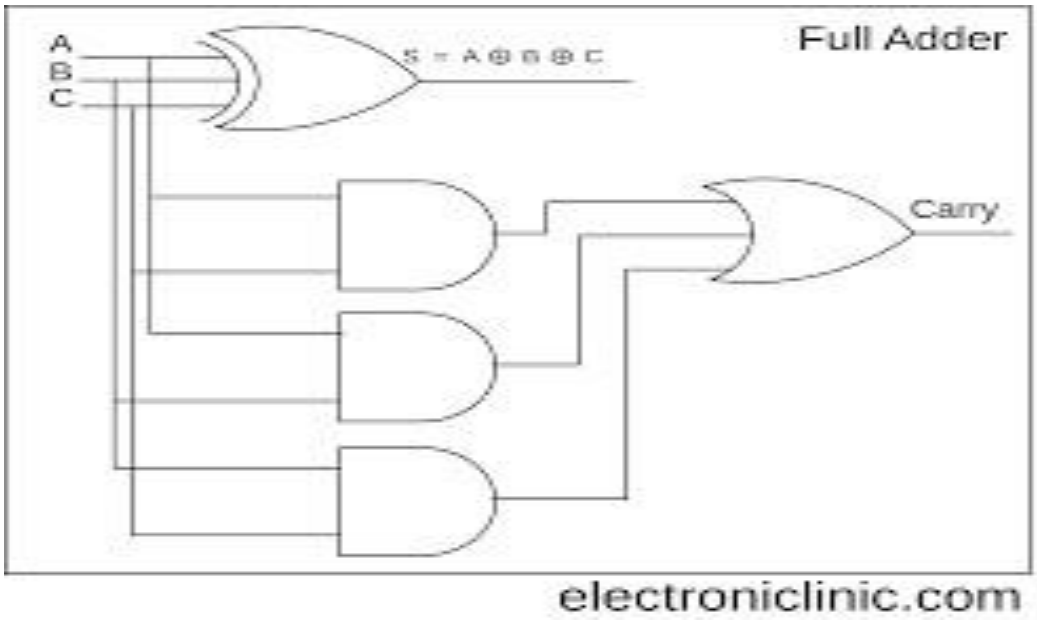
Intput			O tput	
A	B	C	Sum(s)	Carry(c)
1	1	0	0	1
1	1	1	1	1

Logic gate diagram of half adder



HA Logical Diagram

Logic gate diagram of full adder



Aim of the experiment

To study about 4 bit binary to grey code convertor.

Apparatus required

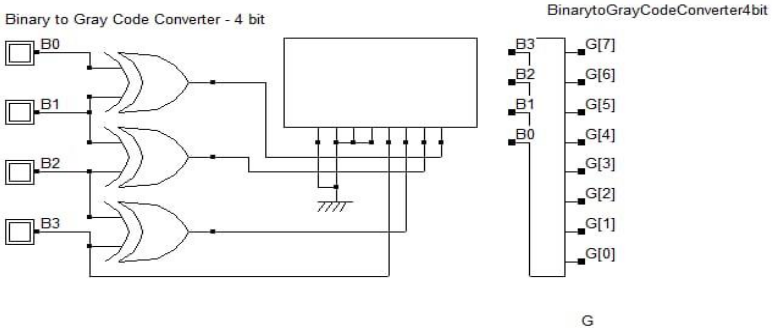
1. Digital trainer kit
2. Probes(connector)
3. Power supply

Truth Table

BINARY CODE				GRAY CODE			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	O	0
1	0	0	0	1	1	O	0
1	0	0	1	1	1	O	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

CONCLUSION-:

->We concluded that the above experiment has done by me.



Aim of the Experiment:-

To study about 2 bit comparator.

Apparatus Required:-

1. Digital trainer kit
2. Probes(Connector)
3. Power Supply

Truth Table:-

TRUTH TABLE

INPUTS				OUTPUTS		
A_2	A_0	B_1	B_0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

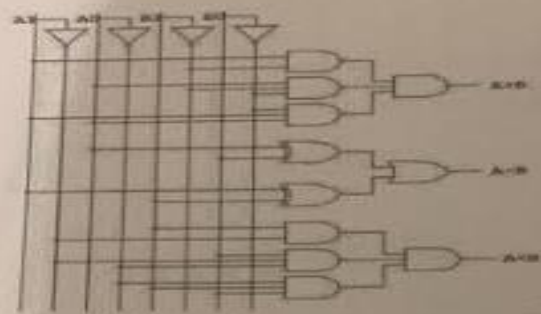
Diagram:-

2) 2- BIT COMPARATOR

$(A>B) = A1\bar{B}1 + A0\bar{B}1\bar{B}0 + \bar{B}0A1A0$

$(A<B) = B1\bar{A}1 + B0\bar{A}1\bar{A}0 + \bar{A}0\bar{B}1\bar{B}0$

$(A=B) = \overline{(A0 \oplus B0)+(A1 \oplus B1)}$



2-bit comparator circuit diagram

Conclusion:-

We concluded that the above experiment has done by me.

Aim of the Experiment:-

To design multiplexer (4:2) and Demultiplexer (1:4)

Apparatus required:-

a. Digital trainer kit
b. Probes (connector)
c. Power supply

Truth table:-

Multiplexer(4:1):

SELECTOR		OUTPUT
S_1	S_2	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Demultiplexer (1:4):-

Input selector output

S_1 S_0 D_0 D_1 D_2 D_3

Conclusion:-

We concluded that the above experiment has been done by us successfully.

EXPERIMENT-14

AIM OF THE EXPERIMNT :-

To decide the operation of flip-flop

(i) S-r flip-flop (ii) j-k flip-flop (iii) d- flip-flop (iv) t- flip-flop

Apparatus required:-
(a)digital trainer kit
(b)probas (connector)
(c)power supply

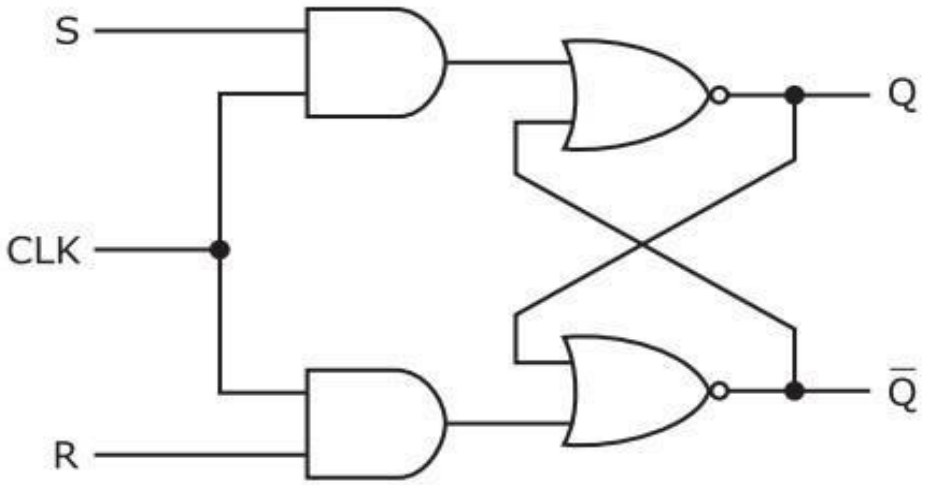
TRUTH TABLE:-

(i) SR flip flop:-

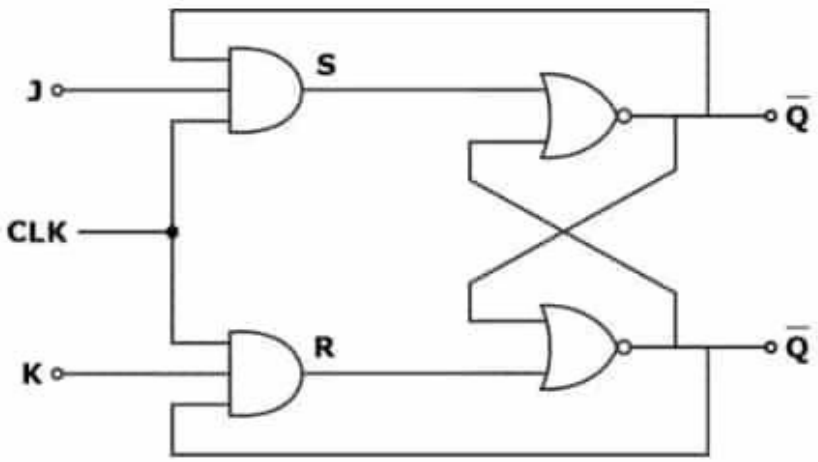
Input			output
Clk	**S**	**R**	**Qn+1x**
0	**x**	**x**	**Qn**
1	**0**	**0**	**Qn**
1	**0**	**1**	**0**
1	**1**	**0**	**1**
1	**1**	**1**	**invalid**

(ii) **J.K flip flop:-**

Input			Output
Clk	**J**	**K**	**Q Q**
O	**X**	**X**	**Memory state**
1	**0**	**0**	**Memory state**
1	**0**	**1**	**0 1**
1	**1**	**0**	**1 0**
1	**1**	**1**	**0 1**



$\boxed{S = J\overline{Q}}$ and $\boxed{R = KQ}$



iii) d- flip flop :-

Clk	D	Qn+1
0	x	Qn
1	0	0
1	1	

iv) t flip flop:-

Clk	T	Q	$\bar{Q}$
0	X	Memory state	
1	0	Memory	
1	1	Memory	

Conlusion:-

We concluded that the above experiment has been done by us succesfully.

EXPERIMENT- 15

AIM OF THE EXPERIMENT :-

To realize about 4 bit asynchronous UP/DOWN counter with a control for up/down counting .

APPARATUS REQUIRED:-

1. Digital trainer kit
2. Probes(connector)
3. Power supply

THEORY :-

Asynchronous counters are a kind of digital circuitry which may count either upwards or downwards while not adhering to the timing pulses from an oscillator. As a result, state transitions are determined by extra inputs rather than by time frames at fixed intervals. The flip-flops and logic gates are utilized for designing the asynchronous counter in order to get counting sequence control based on input signals. With such characteristics they offer flexibility in counting and can be applied in many situations that demands am asynchronous action.

Design of 3 Bit Asynchronous UP/DOWN Counter

It is used more than separate up or down counter.

1. In this a mode control input (say M) is used for selecting up and down mode.

2. A combinational circuit is required between each pair of flip-flop to decide whether to do up or do down counting.

For n = 4, i.e for 4 bit counter –
Maximum count = **2n -1** and number of states are **2n.**

Decision for mode control input

When M = 0, then Y= Q, therefore it will perform Up counting (As discussed above).When M = 1, then Y= Q’ therefore it will perform Down counting (As discussed above).Combinational circuit is required for deciding mode control(i.e., whether counter will perform Up counting or Down counting).

TRUTH TABLE

M	Q	Q'	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Explanation of Up counter

- The 1st FF is connected to logic 1. Therefore, it will toggle for every falling edge.
- The 2nd FF input is connected to Q1.Therefore it changes its state when Q1= 1 and there is falling edge of clock.
- Similarly, 3rd FF is connected to Q2. Therefore, it changes its state when Q2= 1 and there is falling edge of clock.
- By this we can generate counting states of Up counter.
- After every 8th falling edge the counter is again reaching to state 0 0 0. Therefore, it is also known as divide by 8 circuit or mod 8 counter.

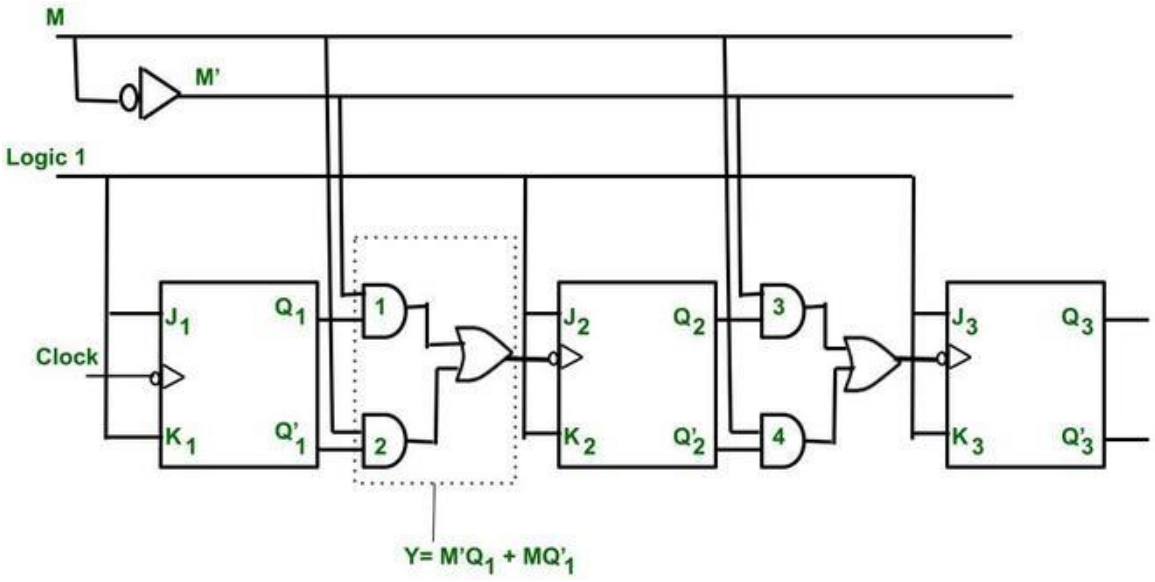
Explanation of Down counter

- The 1st FF is connected to logic 1. Therefore, it will toggle for every falling edge.
- The 2nd FF input is connected to Q'1.Therefore it changes its state when Q'1= 1 and there is falling edge of clock.
- Similarly, 3rd FF is connected to Q'2. Therefore, it changes its state when Q'2= 1 and there is falling edge of clock.
- By this we can generate counting states of down counter.
- After every 8th falling edge the counter is again reaching to state 0 0 0. Therefore, it is also known as divide by 8 circuit or mod 8 counter.

CONCLUSION:-

We concluded that the above experiment has been done by us succesfully.

LOGIC GATE DIAGRAM:-



EXPERIMENT-16

AIM OF THE EXPERIMENT:-

To study about sift registers.

APPARATUS REQUIRED:-

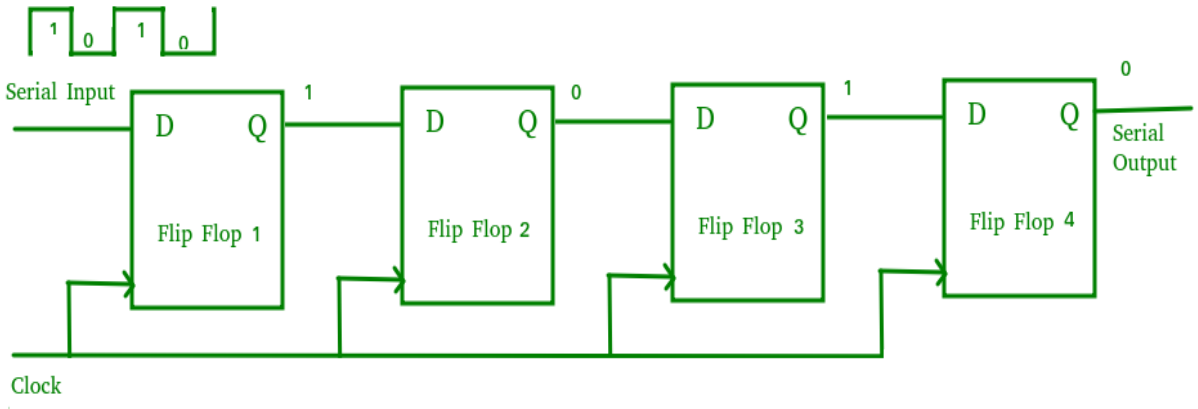
1. Digital Trainer Kit
2. Probes(connector)
3. Power Supply

THEORY:-

1. Serial In Serial Out (SISO):-

   The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as a Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register. The circuit consists of four D flip-flops which are connected in a serial manner.

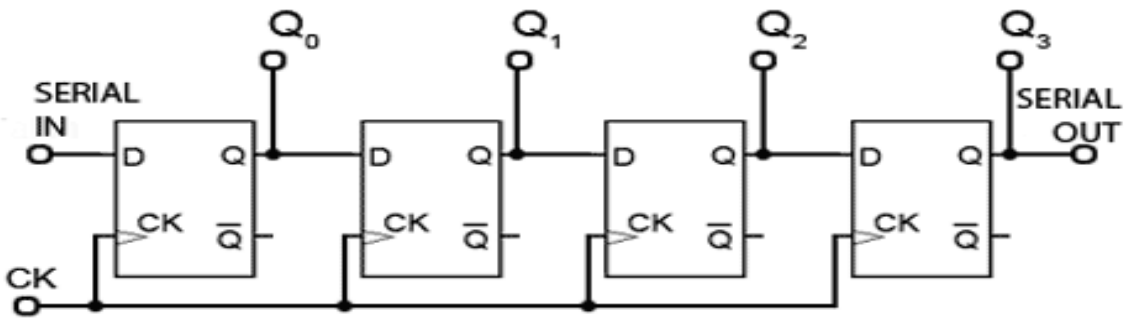
   REGISTER DIAGRAM:-



2. Serial In Parallel Out (SIPO):-

   The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as the Serial-In Parallel-Out shift register. The logic circuit given below shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The output of the first flip-flop is connected to the input of the next flip flop and so on.

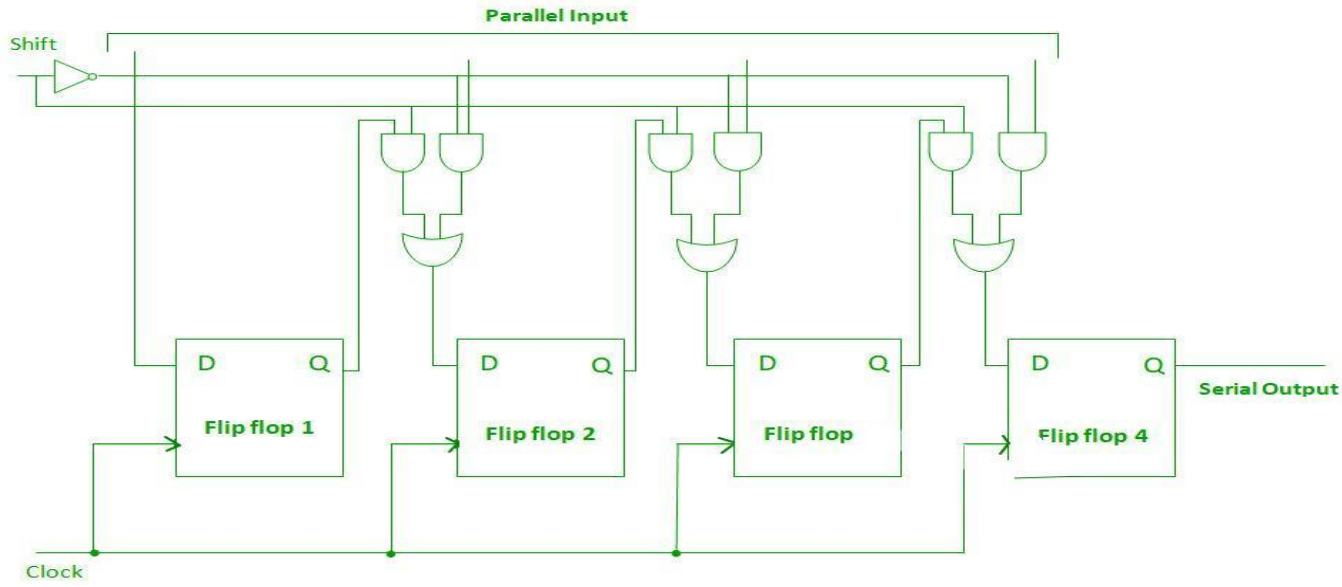
   REGISTER DIAGRAM :-



3. Parallel In Serial Out (PISO) :-

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as a Parallel-In Serial-Out shift register. The logic circuit given below shows a parallel-in-serial-out shift register. The circuit consists of four D flip-flops which are connected. The clock input is directly connected to all the flip-flops but the input data is connected individually to each flip-flop through a multiplexer at the input of every flip-flop. The output of the previous flip-flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip-flop.

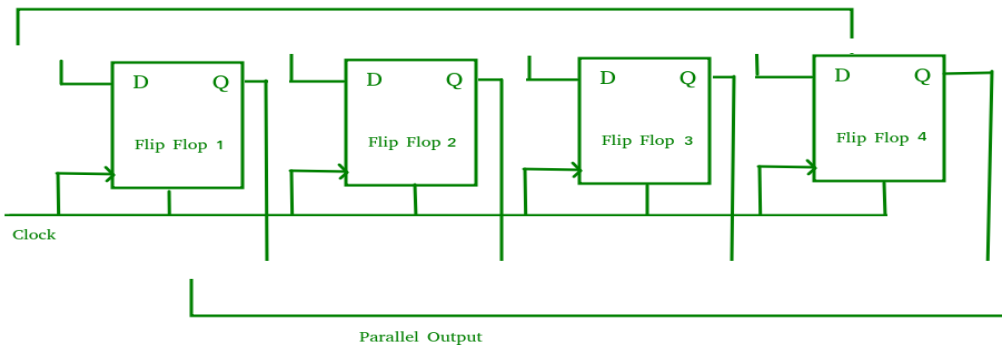
REGISTER DIAGRAM:-



4. Parallel In Parallel Out (PIPO):-

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register. The logic circuit given below shows a parallel-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal and clock signals are connected to all 4 flip-flops. In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required. Data is given as input separately for each flip flop and in the same way, output is also collected individually from each flip flop.

REGISTER DIAGRAM:-



CONCLUSION :-

We concluded that the above experiment has been done by us succesfully.

EXPERIMENT-17

AIM OF THE EXPERIMENT :-

To verify the operations of 8 bit D/A and A/D conversion and test its performance.

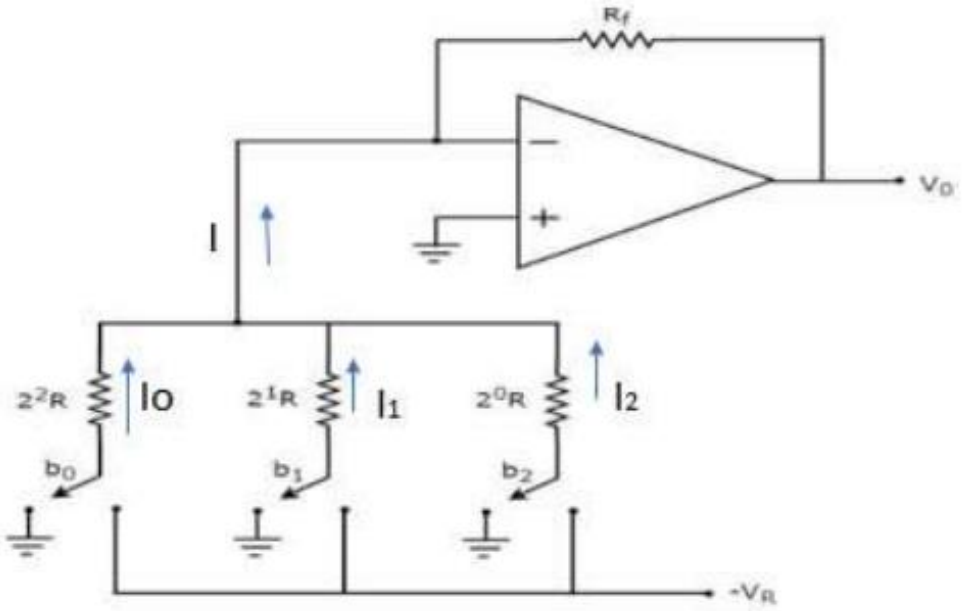
APPARATUS REQUIRED :-

1. Digital Trainer Kit
2. Probes (connector)
3. Power Supply

Digital to Analog Convertor : -

A Digital to Analog Converter (DAC) converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using binary weighted resistors in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC.

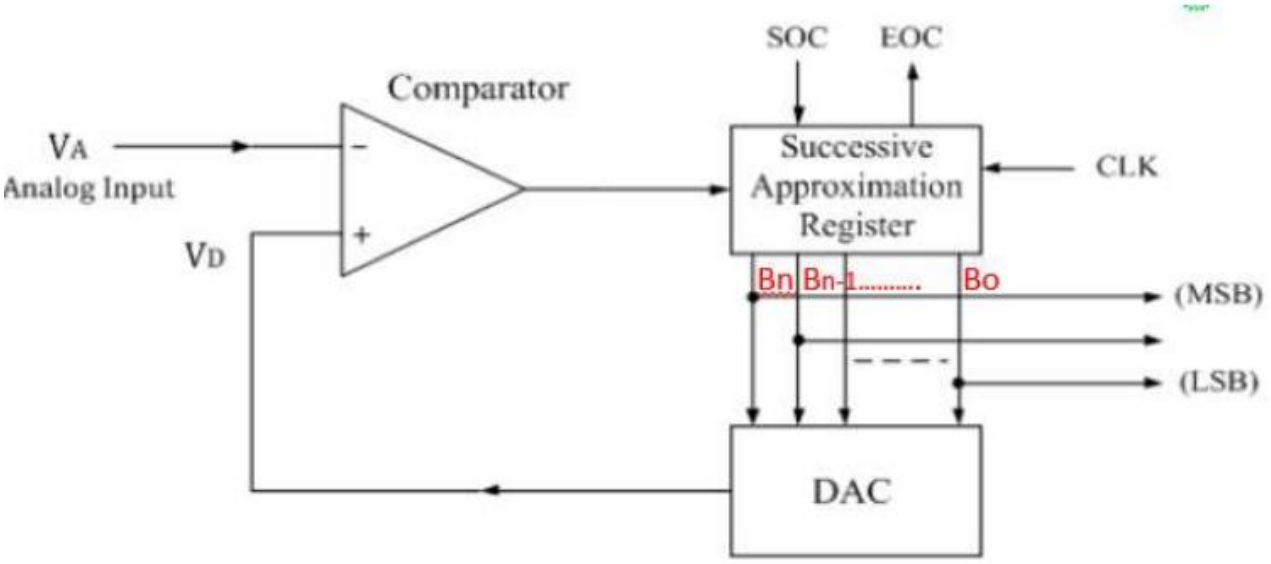
CIRCUIT DIAGRAM:-



Analog to Digital Convertor : -

The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps. It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC. The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR.

CIRCUIT DIAGRAM :-



CONCLUSION :-

We concluded that the above experiment has been done by us succesfully.

EXPERIMENT-18

AIM OF THE EXPERIMENT:-

To study about display devices(LED,LCD,7 SEGMENT DISPLAY).

APPARATUS REQUIRED:-

1. Digital Trainer Kit
2. Probes (Connector)
3. Power supply

1. LED Displays

LED (Light Emitting Diode) displays use an array of LEDs to display images or text. Each LED emits light when an electric current passes through it.

An LED display consists of:

1. LED array: A matrix of LEDs, usually arranged in a 7-segment or dot-matrix configuration.

2. Driver ICs: Integrated circuits that control the LEDs, providing the necessary voltage and current.

3. Microcontroller: A small computer that generates the display data and controls the driver ICs.

Working Principle

1. The microcontroller sends display data to the driver ICs.

2. The driver ICs convert the data into a series of electrical pulses.

3. The pulses are applied to the LED array, causing the corresponding LEDs to emit light.

4. The LEDs are arranged in a pattern to display the desired image or text.

2. LCD Displays

LCD displays use a combination of transistors and capacitors to control the liquid crystals.
LCD (Liquid Crystal Display) displays use a layer of liquid crystals to block or allow light to pass through a matrix of pixels.
Construction
An LCD display consists of:
1. Liquid crystal layer: A thin layer of liquid crystals that can be controlled to block or allow light.
2. Polarizing filters: Filters that polarize the light passing through the liquid crystals.
3. Electrode layer: A layer of electrodes that apply an electric field to the liquid crystals.
4. Backlight: A light source that illuminates the LCD panel.
Working Principle
1. The electrode layer applies an electric field to the liquid crystals.
2. The liquid crystals align themselves according to the electric field.

3. The polarizing filters block or allow light to pass through the liquid crystals.
4. The backlight illuminates the LCD panel, making the images visible.

Truth Table for an LCD Display

No.	LCD Segments							Binary			
No.	In	In	In	In	In	In	In	Out	Out	Out	Out
0	1	1	1	1	1	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	1
2	1	1	0	1	1	0	1	0	0	1	0
3	1	1	1	1	0	0	1	0	0	1	1
4	0	1	1	0	0	1	1	0	1	0	0
5	1	0	1	1	0	1	1	0	1	0	1
6	0	0	1	1	1	1	1	0	1	1	0
7	1	1	1	0	0	0	0	0	1	1	1
8	1	1	1	1	1	1	1	1	0	0	0
9	1	1	1	0	0	1	1	1	0	0	1

3. 7 Segment Display :-

Seven segment displays are the output display device that provides a way to display information in the form of images or text or decimal numbers which is an alternative to the more complex dot matrix displays. It is widely used in digital clocks, basic calculators, electronic meters, and other electronic devices that display numerical information. It consists of seven segments of light-emitting diodes (LEDs) which are assembled like numerical 8. Each segment is labeled with a letter (a to g). The segments are arranged in a specific pattern to display digits from 0 to 9.

Working:-

- a to g represent the 7 segments of the LED display.

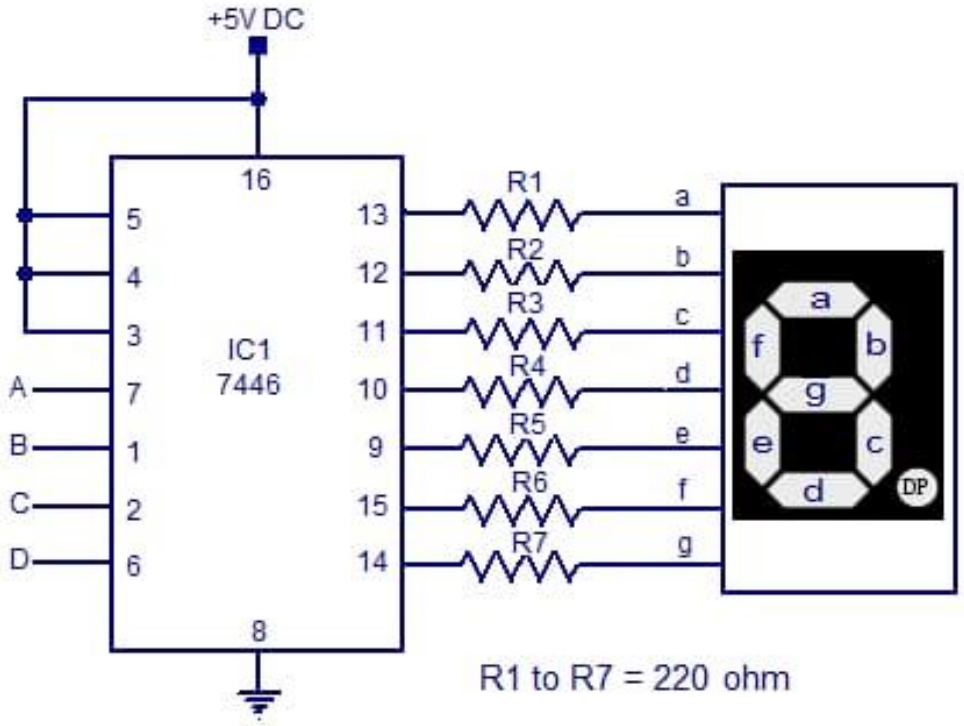
- 1 indicates the segment is ON (emitting light).

- 0 indicates the segment is OFF (not emitting light).

Truth Table for a 7-Segment LED Display

Decimal Digit	Individual Segments Illuminated						
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Logic Gate Diagram:-



CONCLUSION :-

We concluded that the above experiment has been done by us succesfully.