DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGG.

LESSON PLAN

OF

DIGITAL ELECTRONICS LAB (PR.2)

4TH SEMESTER

ACADEMIC YEAR: 2025-26 (SUMMER)

BY

NIRANJAN NAYAK

LECTURER STAGE – II (AE&I)

BHUBANANDA ORISSA SCHOOL OF ENGINEERING

NEAR SCB MEDICAL COLLEGE & HOSPITAL, MANGALABAG, CUTTACK – 753007, ODISHA

Website : https//bosecuttack.org.in

Semester: 4th . DIPLOMA

Session: SUMMER

Subject: DE LAB

No of Period :60(4p/week)

Branch: AE&I

Name of Faculty: Niranjan Nayak

Period	Week	Date	Topics to be Covered
1	1	22.12.2025	To verify the truth tables for all logic fates – NOT OR AND NAND NOR XOR XNOR using CMOS Logic gates and TTL Logic Gates.
2			
3		23.12.2025	To verify the truth tables for all logic fates – NOT OR AND NAND NOR XOR XNOR using CMOS Logic gates and TTL Logic Gates.
4			
5	2	29.12.2025	Implement and realize Boolean Expressions with Logic Gates.
6			
7		30.12.2025	Implement and realize Boolean Expressions with Logic Gates.
8			
9	3	05.01.2026	Implement Half Adder, Full Adder using ICs.
10			
11		06.01.2026	Implement Half Adder, Full Adder using ICs.
12			
13	4	12.01.2026	Implement Half Subtractor, Full subtractor using ICs.
14			
15		13.01.2026	Implement Half Subtractor, Full subtractor using ICs.
16			
17	5	19.01.2026	Implement parallel and serial full-adder using ICs.
18			
19		20.01.2026	Implement parallel and serial full-adder using ICs.
20			
21	6	02.02.2026	Design and development of Multiplexer and De-multiplexer using multiplexer ICs
22			
23		03.02.2026	Design and development of Multiplexer and De-multiplexer using multiplexer ICs
24			
25	7	09.02.2026	Verification of the function of SR,D, JK and T Flip Flops.
26			

27		10.02.2026	Verification of the function of SR,D, JK and T Flip Flops.
28			
29	8	16.02.2026	Design controlled shift registers.
30			
31		17.02.2026	Design controlled shift registers.
32			
33	9	23.02.2026	Construct a Single digit Decade Counter (0-9) with 7 segment display.
34			
35		24.02.2026	Construct a Single digit Decade Counter (0-9) with 7 segment display.
36			
37	10	02.03.2026	To design a programmable Up-Down Counter with a 7 segment display.
38			
39	11	09.03.2026	To design a programmable Up-Down Counter with a 7 segment display.
40			
41		10.03.2026	Study of different memory ICs.
42			
43	12	16.03.2026	Study of different memory ICs.
44			
45		17.03.2026	Study Digital- to – Analog and Analog to Digital Converters.
46			
47	13	23.03.2026	Study Digital- to – Analog and Analog to Digital Converters.
48			
49		24.03.2026	Simulate in Software (such as PSpice) an Analog to Digital Converter
50			
51	14	30.03.2026	Simulate in Software (such as PSpice) an Analog to Digital Converter
52			

53		31.03.2026	Simulate in Software (such as PSpice) an Digital to Analog Converter
54			
55	15	06.04.2026	Simulate in Software (such as PSpice) an Digital to Analog Converter
56			
57		07.04.2026	**VIVA**
58			
59	16	13.04.2026	**VIVA**
60			

Signature Of Faculty

Signature of HOD