BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF INFORMATION TECHNOLOGY
LESSON PLAN

Discipline: IT	Semester: 3rd	No. Of period available	Name of the Teaching Faculty: Bhabodeepika Mohanty
Subject: DE	No. Of Days/per week class allotted: 4 periods per week (Mon,Tue,Thu,Fri)		From Date 01-08-2023 To Date: 30-11-2023 No. Of Weeks: 18 weeks
WEEK	**CLASS DAY**		**Topics to be covered**
1st	01.08.23	1	**Unit-1: Basics of Digital Electronics** Introduction
	03.08.23	1	1.1Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system.
	04.08.23	1	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1" s & 2" s complement of Binary numbers& Subtraction using complements method
2nd	07.08.23	1	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1" s & 2" s complement of Binary numbers& Subtraction using complements method
	08.08.23	1	1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes excess-3 and Gray codes.
	10.08.23	1	1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes excess-3 and Gray codes.
	11.08.23	1	1.4 Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram
3rd	14.08.23	1	1.4 Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram
	17.08.23	1	1.5 Universal Gates& its Realisation
	18.08.23	1	1.6 Boolean algebra, Boolean expressions
4th	21.08.23	1	Demorgan's Theorems. **Assignment-1**
	22.08.23	1	1.7 Represent Logic Expression: SOP & POS forms
	24.08.23	1	1.8 Karnaugh map (3 & 4 Variables)&Minimization of logical expressions
	25.08.23	1	1.8 k-map (don't care conditions) **Class Test-1**

5th	28.08.23	1	**Unit-2: Combinational Logic Circuits** 2.1 Half adder
	29.08.23	1	2.1 Full adder
	31.08.23	1	Half Subtractor
	01.09.23	1	Full Subtractor
6th	04.09.23	1	Serial and Parallel Binary 4 bit adder.
	05.09.23	1	2.2 Multiplexer (4:1)
	07.09.23	1	De- multiplexer (1:4)
	08.09.23	1	Decoder, Encoder
7th	11.09.23	1	Digital comparator (3 Bit)
	12.09.23		2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
	14.09.23	1	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above) **Assignment -2**
	15.09.23	1	Digital comparator (3 Bit)
8th	18.09.23	1	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
	21.09.23	1	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above) **Assignment -2**
	22.09.23	1	**Unit-3: Sequential logic Circuits** 3.1 Principle of flip-flops operation, its Types
9th	25.09.23	1	3.1 Principle of flip-flops operation, its Types
	26.09.23	1	**Class Test-2**
	28.09.23	1	3.2 SR Flip Flop using NAND,NOR Latch (un clocked)
10th	03.10.23	1	3.2 SR Flip Flop using NAND,NOR Latch (un clocked)
	05.10.23	1	3.3 C l o c k e d SR,D, flip-flops-Symbol, logic Circuit, truth table and applications
	06.10.23	1	3.3 C l o c k e d JK,T, flip-flops-Symbol, logic Circuit, truth table and applications

11th	09.10.23	1	Internal Test
	10.10.23	1	Internal Test
	12.10.23	1	3.3 C lo ck ed Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	13.10.23	1	3.4 Concept of Racing and how it can be avoided. **Assignment -3**
12th	16.10.23	1	**Unit-4: Registers, Memories & PLD** 4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
	17.10.23	1	4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
	19.10.23	1	4.2 Universal shift registers-Applications.
	20.10.23	1	4.3 Types of Counter & applications
13th	21.10.23 to 28.10.23		Puja Holiday
14th	30.10.23	1	4.4 Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter.
	31.10.23	1	4.4 Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter.
	02.11.23	1	Synchronous counter, Ring Counter.
	03.11.23	1	4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
15th	06.11.23	1	4.6 Basic concept of PLD & applications
	07.11.23	1	**Unit-5: A/D and D/A Converters** 5.1 Necessity of A/D and D/A converters.
	09.11.23	1	5.2 D/A conversion using weighted resistors methods.
	10.11.23	1	5.3 D/A conversion using R-2R ladder (Weighted resistors) network. **Assignment -4**
16th	13.11.23	1	5.4 A/D conversion using counter method
	14.11.23	1	5.5 A/D conversion using Successive approximate method
	16.11.23	1	**Unit-6: LOGIC FAMILIES** 6.1 Various logic families &categories according to the IC fabrication process
	17.11.23		6.1 Various logic families &categories according to the IC fabrication process

17th	20.11.23		6.2 Characteristics of Digital ICs- Propagation Delay
	21.11.23		fan-out, fan-in, Power Dissipation ,
	23.11.23		Noise Margin ,Power Supply requirement & Speed with Reference to logic families
	24.11.23		6.3 Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR)
18th	28.11.23		REVISION
	30.11.23		PREVIOUS YEAR QUESTION DISCUSSION