BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING

LESSON PLAN

SUBJECT: MICROPROCESSOR AND ITS INTERFACING

ACADEMIC SESSION: 2026-27

FACULTY: SMT RASHMITA GOUDA, LECTURER(STAGE-I)

SEMESTER: 5th

H O D (AE&I)
AE & I Department
B.O.S.E, Cuttack-753007

BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING
LESSON PLAN

COURSE OUTCOMES

After completion of course the student will be able to

CO1: Explain the architecture of 8085 microprocessor

CO2:- Remember the instruction set and write different assembly language program for 8085 Microprocessor

CO3:-. Understand Memory control signals for Read and write cycles and Memory interfacing

CO4:- Understand I/O interfacing, architecture of 8255 PPI and data transfer schemes

CO5:- Explain different types of interrupts and DMA

BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING
LESSON PLAN

Discipline: AE&I Engineering	**Semester: 5th**	**Name of the teaching faculty: Rashmita Gouda**
Subject: Microprocessor & its Interfacing	**No. of Days/ per week class allotted: 03 periods per week.**	**Semester From Date: 01-07-2026 To Date: 05-11-2026 No. of weeks:19**
Week	**Class Day**	**Topics to be covered**
1	1st	**Unit-I:** Architecture of 8085 Microprocessor **Introduction**
	2nd	Functional Block Diagram
2	1st	Registers
	2nd	ALU, Bus systems
	3rd	Timing and control signals,
3	1st	Machine cycles
	2nd	Timing diagrams
4	1st	Revision Unit-I
	2nd	**Unit-II: Programming of 8085 Introduction**
	3rd	Instruction formats
5	1st	Addressing modes

BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING
LESSON PLAN

	2nd	Addressing modes
	3rd	Instruction set
6	1st	Instruction set
	2nd	Need for Assembly language – Development of Assembly language programmes
	3rd	Revision Unit-II
7	1st	**Unit-III: Memory Interfacing** **Introduction**
	2nd	Interface requirements
	3rd	Address space partitioning
8	1st	Buffering of Buses- timing constraints
	2nd	Memory control signals – Read and write cycles
	3rd	Interfacing SRAM, EPROM and DRAM sections
9	1st	Revision Unit-III
10	1st	**Unit-IV: I/O Interfacing** **Introduction**
	2nd	Memory mapped I/O Scheme – I/O mapped I/O scheme
	3rd	Input and Output cycles

BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING
LESSON PLAN

11	1st	Simple I/O ports
	2nd	Programmable peripheral interface (8255)
	3rd	Programmable peripheral interface (8255)
12		
13	1st	Data transfer schemes: Programmable data transfer, DMA data transfer
	2nd	Synchronous, Asynchronous and interrupt driven data transfer schemes
	3rd	Interfacing – Simple keyboards and
14	1st	Interfacing - LED displays
	2nd	Revision Unit-IV
	3rd	**Unit-V: Interrupts and DMA** **Introduction**
15	1st	Interrupt feature, Need for interrupts
	2nd	Characteristics of Interrupts, Types of Interrupts
	3rd	Interrupt structure
16	1st	Methods of servicing interrupts
	2nd	Development of Interrupt service subroutines

BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING
LESSON PLAN

	3rd	Multiple interrupt request and their handling
17	1st	Need for direct memory access
	2nd	Devices for Handling DMA – Programmable DMA controller 8237
18	1st	Programmable DMA controller 8237
	2nd	Revision Unit-V
	3rd	**Probable Q& A discussion**
19	1st	**Probable Q& A discussion**
	2nd	**Probable Q& A discussion**
	3rd	**Probable Q& A discussion**

30/12/2022

Signature of Faculty

HOD (AE&I)

HOD
AE & I Department
B.O.S.E, Cuttack-753007