Unit - 3

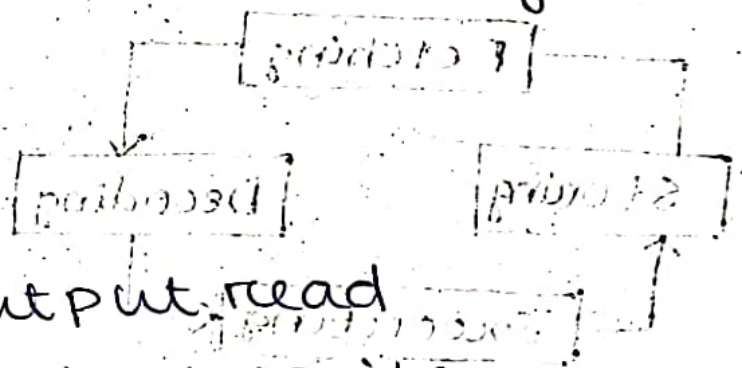
Timing Diagrams

→ The necessary step, which are carried out in machine cycle can be represented graphically such graphically representation is known as timing diagram.

Machine Cycle :- It is defined as the time required to complete one operation of accessing memory, accessing i/p & o/p data etc.

There are 5 types of machine cycle.

(i) Opcode fetch
(ii) Memory read
(iii) Memory write
(iv) Input read / Output read
(v) Input write / Output write



T-State :- It is defined as one subdivision of operation perform in an one clock period.

→ $T\text{-}State = \frac{1}{f}$

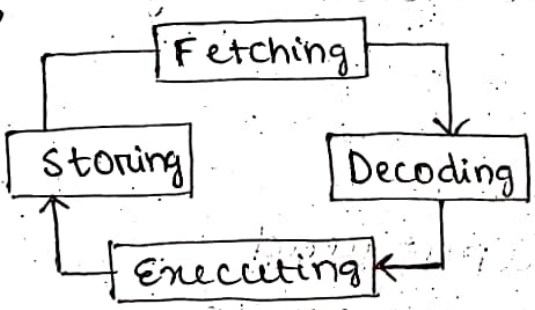
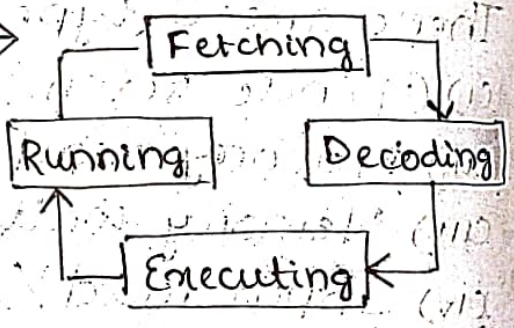
Where, f = clock frequency

→ It is fully depends upon the clock frequency.

→ Each t-state = one clock period.

Fetch cycle :- It is a standard process which is needed for processing of a data. It is called fetch cycle.
It is also known as fetch decode execute cycle.

Instruction Cycle :- It is the time taken to compute the execution of an instruction. It is a combination of fetch cycle & execution cycle.

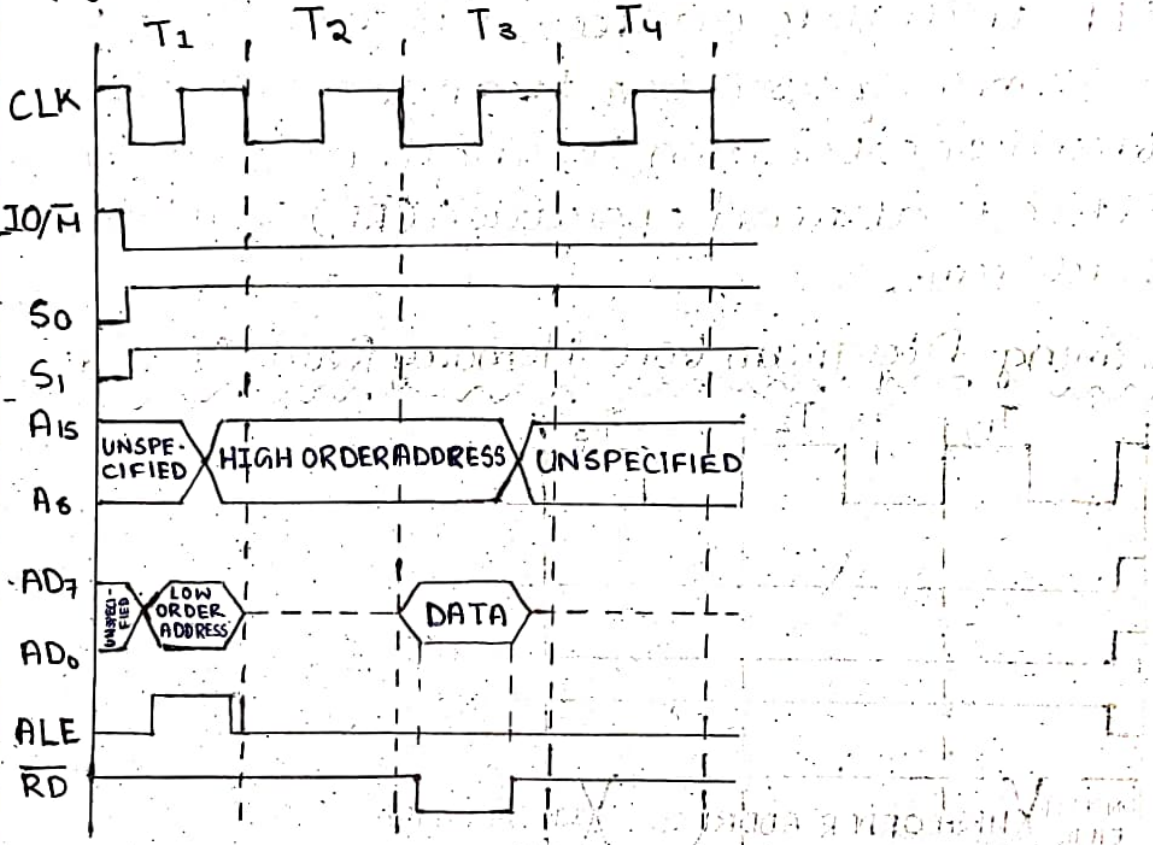
* Machine Cycle	Instruction Cycle
→ It is defined as the time required to complete one operation to accessing memory, accessing i/p, o/p data.	→ It is the time taken to compute the execution of an instruction. It is the combination of FC & EC.
→ 	→ 
→ Process: fetching → Decoding → executing → Storing	→ Process fetching → Decoding → Executing → running

→ It does have memory capability. → Component :- memory unit, CPU → It considering more memory space than IC.	→ It doesn't have memory capability. → Component : Register, ALU. → It considers less memory space than MC.

→ Clock Cycle Speed / clock rate :-

The speed of a computers CPU is determined by clock cycle. The clock rate is measured in Hz.

Timing diagram for Opcode Fetch :-



Description

→ In a fetch cycle, the microprocessor fetches the opcode of an instruction from the memory & above timing diagram for an opcode fetch cycle.

→ T_1, T_2, T_3, T_4 timing diagram for an opcode fetch cycle. T_1, T_2, T_3, T_4 are consecutive 4 clock cycle.

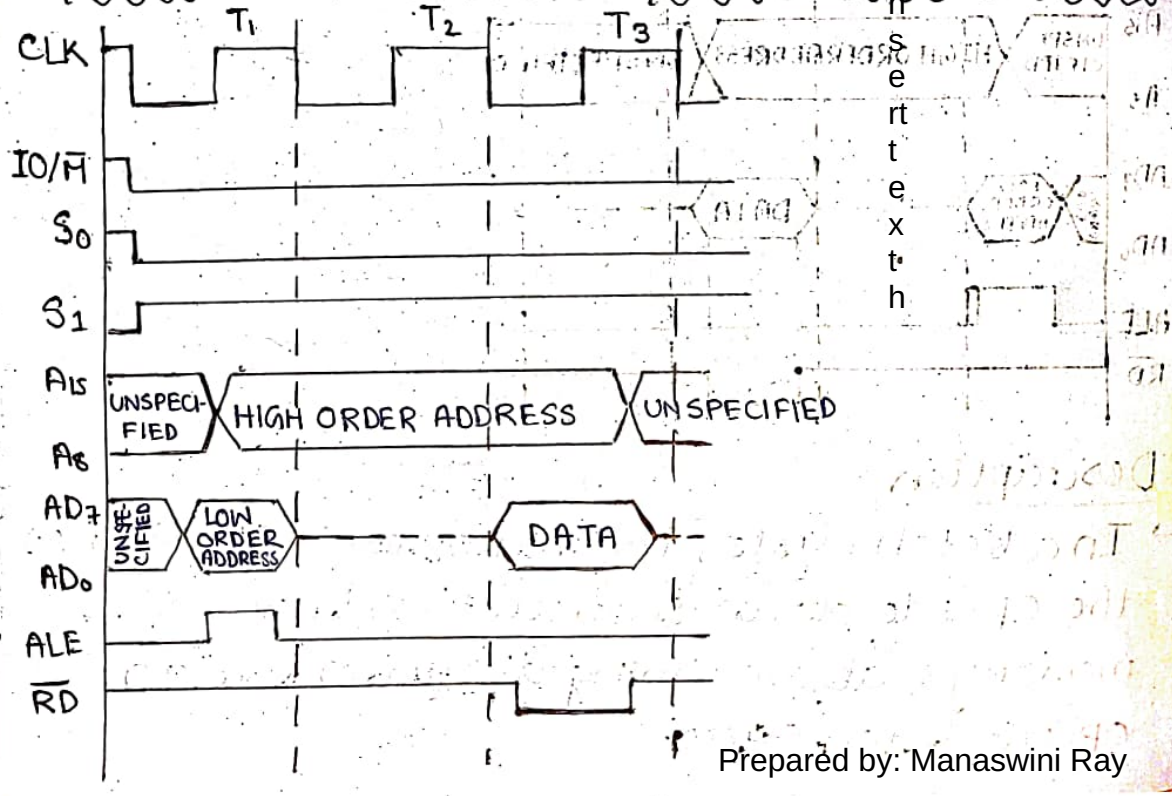
→ The microprocessor issues a low $IO/\overline{M}$ signal to indicate that its want to make communication with the memory.

→ Again the microprocessor sends out high S_0 & S_1 signal to indicate that it is going to perform fetch operation.

→ $A_8 - A_{15}$, $AD_0 - AD_7$ depends upon the data which will be carried out on the opcode fetch cycle.

→ ALE transfer address latch enable & it is mainly used for transfer the data from one location to another location. After that read operation ($\overline{RD}$) will be perform.

Timing Diagram for Memory Read Operation



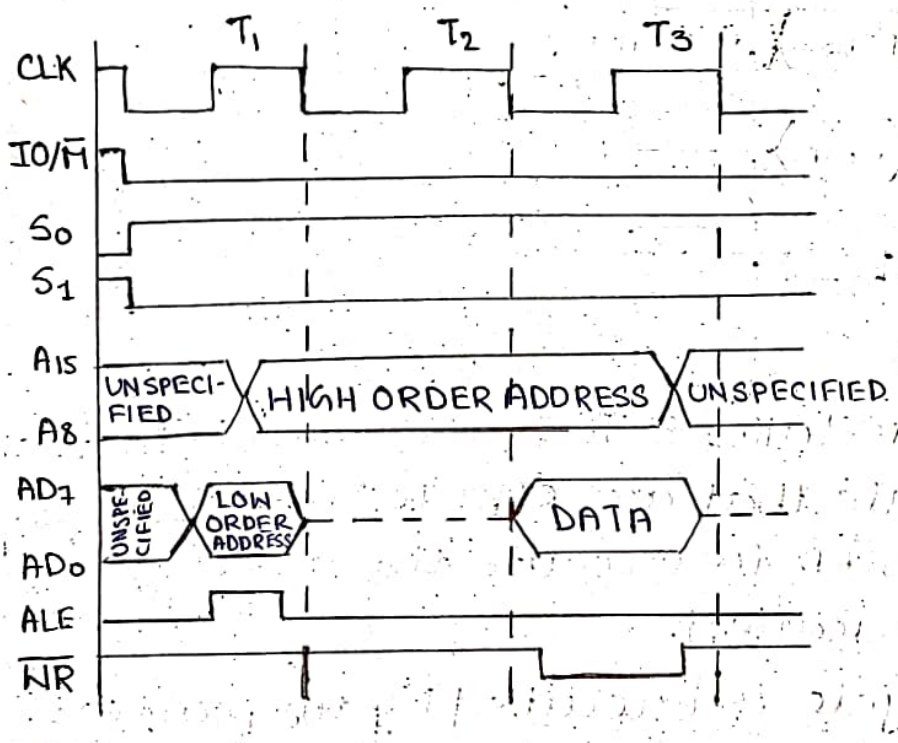
Description

→ The processor takes 3 T-state to execute the cycle for memory read operation & 7 signals are used to read the memory operation & that are CLK, IO/$\overline{M}$, S_0, S_1, A_8 - A_{15}, AD_0 - AD_7, ALE, $\overline{RD}$.

→ The memory read machine cycle is executed by the process and to used to read a data byte from memory.

→ The instruction which have more than 1 byte word size will use this machine cycle after the opecode fetch machine cycle.

Timing Diagram for memory write Operation



Description

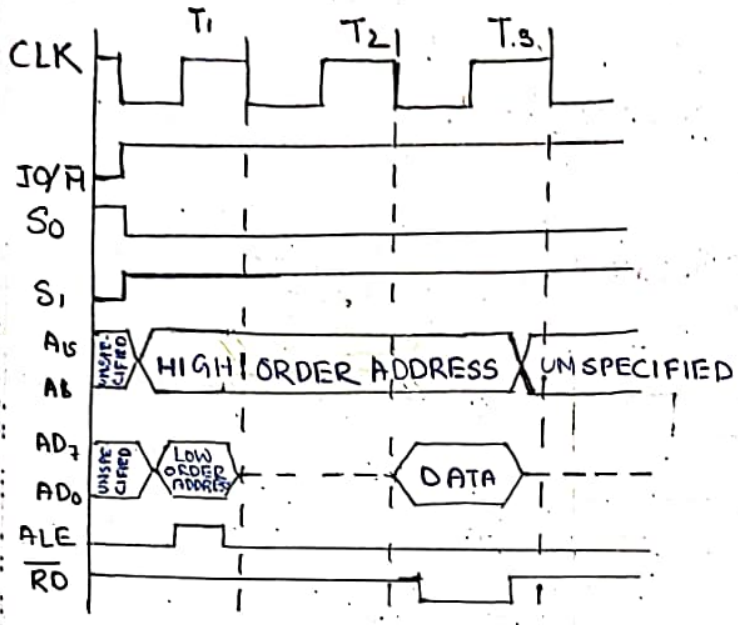
→ The processor takes 3 T-state that is T_1, T_2 T_3 to execute the cycle for memory write operation & 7 signals are used to write the memory operation & that are CLK, IO/$\overline{M}$,

S_0, S_1, $A_8 - A_{15}$, $AD_0 - AD_7$, ALE, $\overline{WR}$.

→ The memory write machine cycle is executed by the processor to write a data byte from memory.

→ The instruction which have more than 1 byte word size will use this machine cycle after the opcode fetch machine cycle.

Timing Diagram for I/O Read Cycle



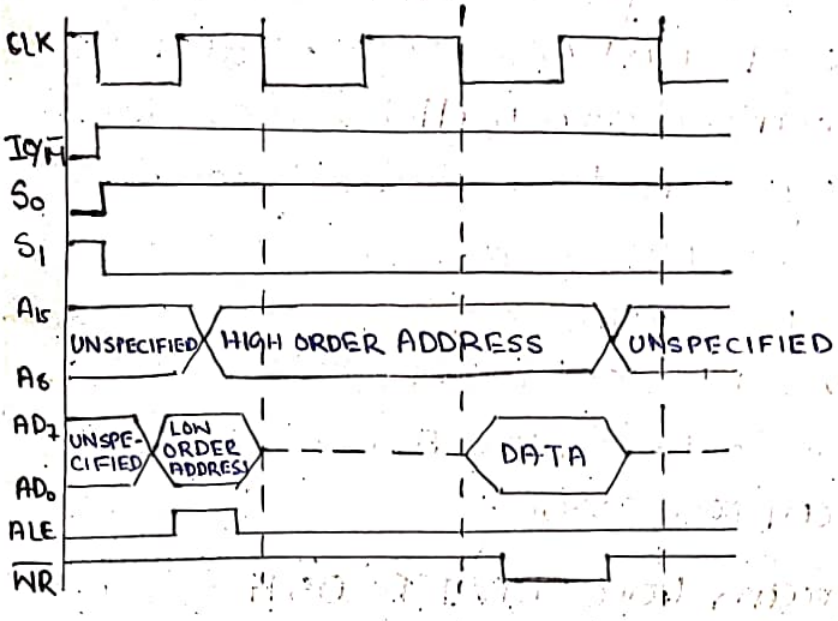
Description

→ The processor takes 3 T-states that is T_1, T_2, T_3 & 7 signals that are CLK, IO/$\overline{M}$, S_0, S_1, $A_8 - A_{15}$, $AD_0 - AD_7$, ALE, $\overline{RD}$ to execute the cycle for I/O read operation.

→ I/O read cycle is executed by the processor to read a data byte I/O port or from the peripheral / which is I/O, mapped in the system.

→ The i/p instruction uses the machine cycle during the execution.

Timing Diagram for I/O write cycle



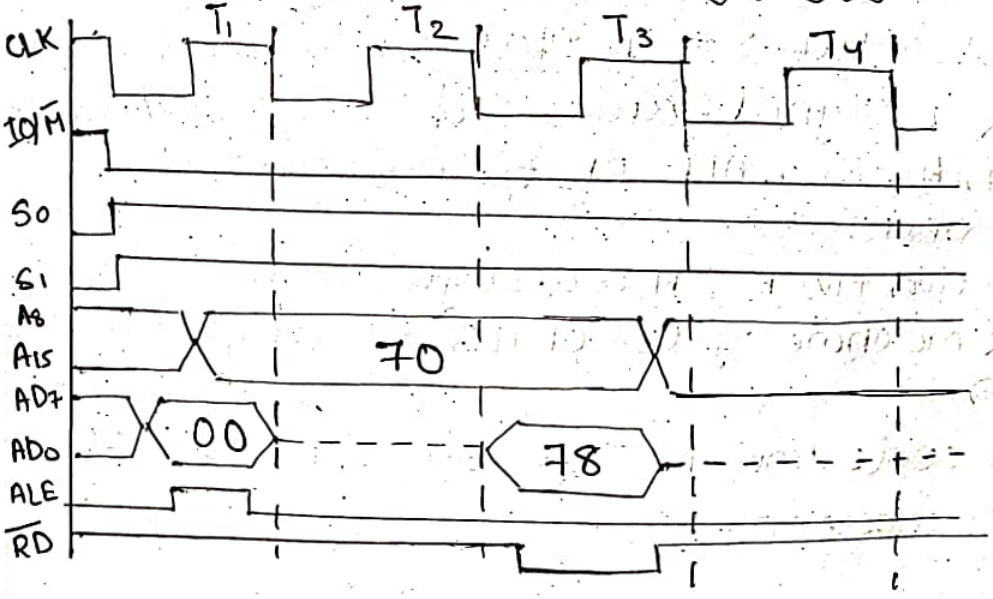
Description

→ The processor takes 3 T-states i.e, T_1, T_2, T_3 & 7 signals i.e, CLK, IO/M, S_0, S_1, AD_0- AD_7, A_8 - A_{15}, ALE, $\overline{WR}$.

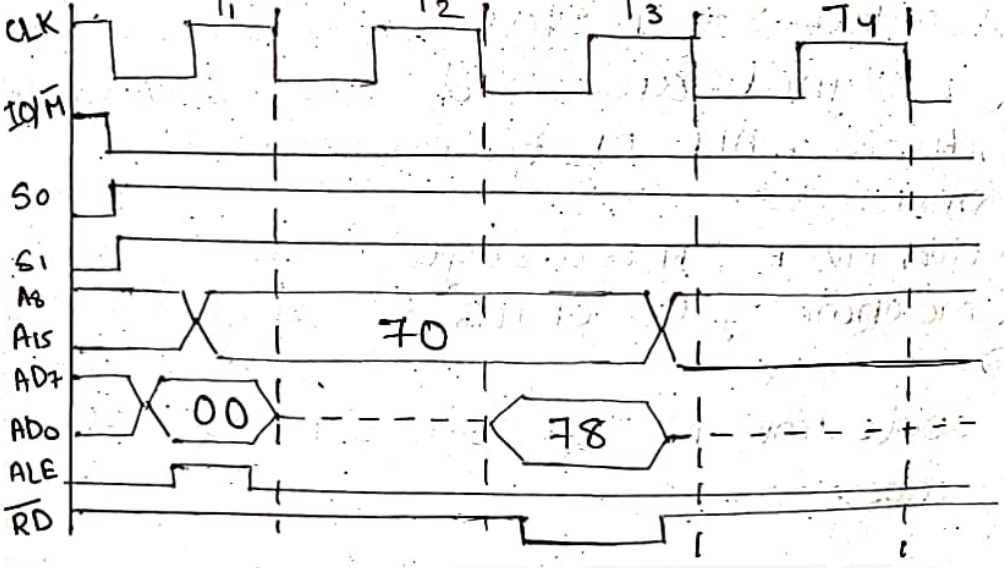
→ I/O write cycle is executed by the process of write a data byte I/O port or from the peripheral or which is I/O mapped in the system.

→ The i/p instruction uses the machin cycle during the execution.

Timing Diagram for MOV A,B



Prepared by:
Manaswini Ray

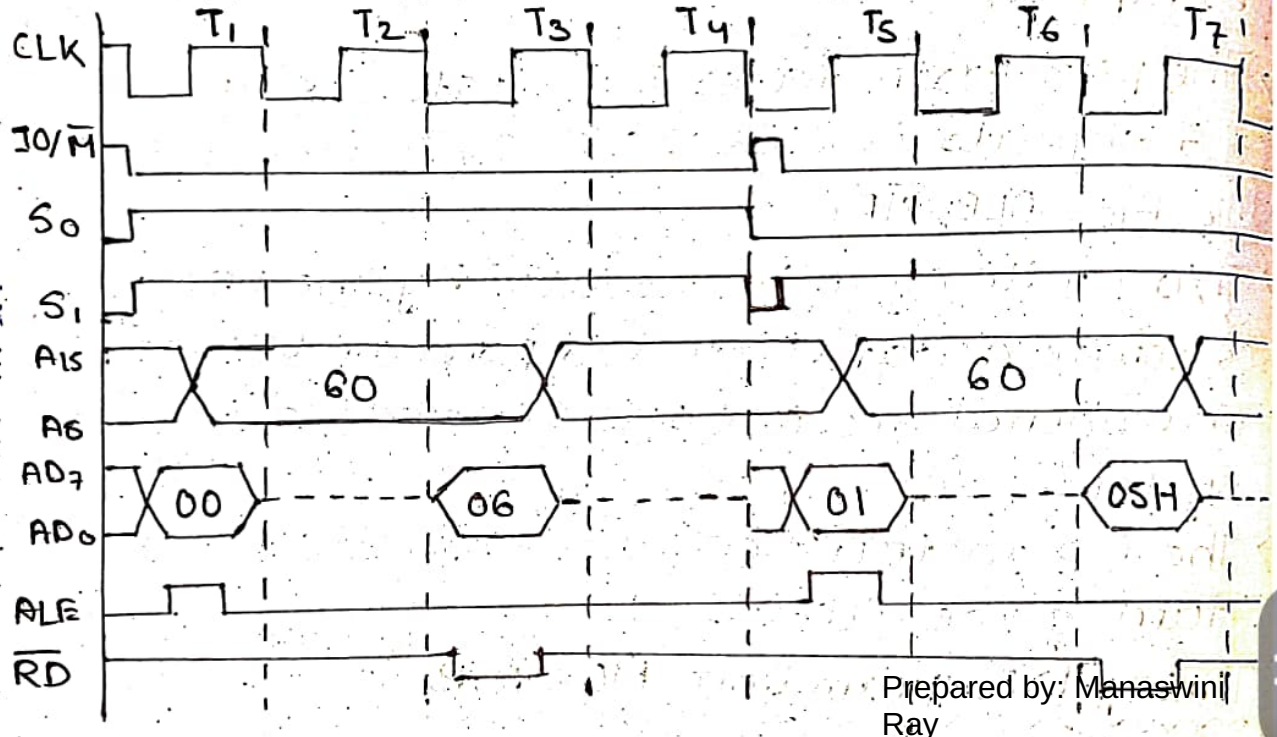


→ The processor takes [illegible] i.e T_1, T_2, T_3, T_4 & 7 signals are used to execute the operation such that MOV A, B that means data will be move from B-C pair register to accumulator.

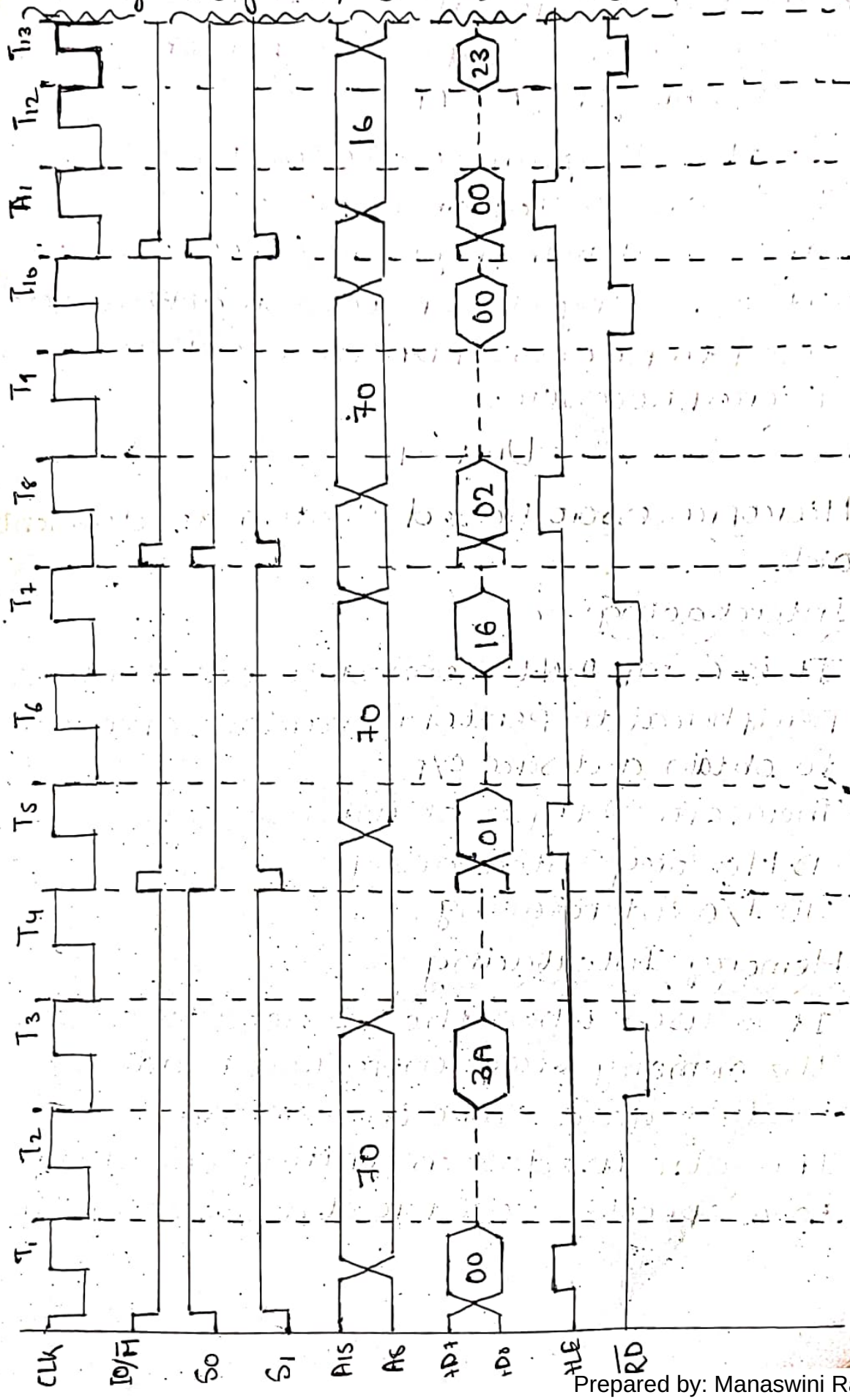
→ The instruction MOV A, B is a 1 byte instruction, mp takes one machin cycle (opcode fetch) to complete instruction.

→ Hence, the code for MOV A, B is passed to the microprocessor.

Timing Diagram for MVI B, 05H



Timing Diagram for LDA 1600H



→ The processor takes 13 T-state i.e, T_1 to T_{13} 7 signals are used i.e. CLK, ALE, $\overline{RD}$, IO/$\overline{M}$ S_0, S_1, AD_0 - AD_7, A_8 - A_{15}.

→ In this diagram, we follow that T_1, T_2, T_3, T_4 are called opcode fetch & T_5 - T_{13} are called memory read / opcode read.

→ It consisting of 3 bytes, 4 machine cycle used to process LDA instruction in microprocessor.

Unit - 4