BHUBANANANDA ODISHA SCHOOL OF ENGINEERING, CUTTACK
DEPARTMENT OF Computer Science & Engineering
LESSON PLAN

Discipline: CSE	Semester: 3rd	No. Of period available	Name of the Teaching Faculty: Sonalisa Behera
Subject: DE	No. Of Days/per week class allotted: 4 periods per week (Mon,Tue,Thu,Fri)		From Date 15-09-2022 To Date: 22-12-2022 No. Of Weeks: 15 weeks
WEEK	**CLASS DAY**		**Topics to be covered**
1st	15.09.22	1	**Unit-1: Basics of Digital Electronics** Introduction
	16.09.22	1	1.1Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system.
2nd	19.09.22	1	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1"s & 2"s complement of Binary numbers& Subtraction using complements method
	20.09.22	1	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1"s & 2"s complement of Binary numbers& Subtraction using complements method
	22.09.22	1	1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes excess-3 and Gray codes.
	23.09.22	1	1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes excess-3 and Gray codes.
3rd	26.09.22	1	1.4 Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram
	27.09.22	1	1.4 Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram
	29.09.22	1	1.5 Universal Gates& its Realisation
	30.09.22	1	1.6 Boolean algebra, Boolean expressions,
4th	03.10.22 to 08.10.22		Puja Holiday

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5th	10.10.22	1	Demorgan"s Theorems. **Assignment-1**
	11.10.22	1	1.7 Represent Logic Expression: SOP & POS forms
	13.10.22	1	1.8 Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,
	14.10.22	1	1.8 k-map (don"t care conditions) **Class Test-1**
6th	17.10.22	1	**Unit-2: Combinational Logic Circuits** 2.1 Half adder,
	18.10.22	1	2.1, Full adder,
	20.10.22	1	Half Subtractor,
	21.10.22	1	Full Subtractor
7th	25.10.22	1	Serial and Parallel Binary 4 bit adder.
	27.10.22	1	2.2 Multiplexer (4:1),
	28.10.22	1	De- multiplexer (1:4),
8th	31.10.22	1	Decoder, Encoder,
	01.11.22	1	Digital comparator (3 Bit)
	03.11.22	1	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
	04.11.22	1	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above) **Assignment -2**
9th	07.11.22	1	**Unit-3: Sequential logic Circuits** 3.1 Principle of flip-flops operation, its Types,
	10.11.22	1	3.1 Principle of flip-flops operation, its Types,
	11.11.22	1	**Class Test-2**
10th	14.11.22	1	**Internal Test**
	15.11.22	1	**Internal Test**
	17.11.22	1	3.2 SR Flip Flop using NAND,NOR Latch (un clocked)
	18.11.22	1	3.2 SR Flip Flop using NAND,NOR Latch (un clocked)

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11th	21.11.22	1	3.3 Clocked SR,D, flip-flops-Symbol, logic Circuit, truth table and applications
	22.11.22	1	3.3 Clocked JK,T, flip-flops-Symbol, logic Circuit, truth table and applications
	24.11.22	1	3.3 Clocked Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	25.11.22	1	3.4 Concept of Racing and how it can be avoided. **Assignment -3**
12th	28.11.22	1	**Unit-4: Registers, Memories & PLD** 4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
	29.11.22	1	4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
	01.12.22	1	4.2 Universal shift registers-Applications.
	02.12.22	1	4.3 Types of Counter & applications
13th	05.12.22	1	4.4 Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter.
	06.12.22	1	4.4 Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter.
	08.12.22	1	Synchronous counter, Ring Counter.
	09.12.22	1	4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
14th	12.12.22	1	4.6 Basic concept of PLD & applications
	13.12.22	1	**Unit-5: A/D and D/A Converters** 5.1 Necessity of A/D and D/A converters.
	15.12.22	1	5.2 D/A conversion using weighted resistors methods.
	16.12.22	1	5.3 D/A conversion using R-2R ladder (Weighted resistors) network. **Assignment -4**
15th	19.12.22	1	5.4 A/D conversion using counter method
	20.12.22	1	5.5 A/D conversion using Successive approximate method
	22.12.22	1	**Unit-6: LOGIC FAMILIES** 6.1 Various logic families &categories according to the IC fabrication process
			6.1 Various logic families &categories according to the IC fabrication process

			6.2 Characteristics of Digital ICs- Propagation Delay
			fan-out, fan-in, Power Dissipation ,
			Noise Margin ,Power Supply requirement &Speed with Reference to logic families
			6.3 Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR)