Experiment - 1

AIM OF THE EXPERIMENT:

Introduction to digital electronics.

DEFINATION OF DIGITAL ELECTRONICS:

i) Digital electronics is a branch of electronics that deals with two digits i.e. 0 & 1.Here, 0 means low logic or false and 1 means high logic or true.
ii) Digital electronics involving study about the digital signal use and produce them.
iii) Digital electronics operates to including different types of gates and that gates are binding with integral circuit.

REQUIREMENTS TO CONDUCT DIGITAL ELECTRONICS LAB:

a) Digital electronics trainer kit.
b) Power connection.
c) Connector
d) Gloves

ADVANTAGES OF DIGITAL ELECTRONICS:

a) Digital systems are easier to design.
b) Information storage is easy.
c) Accuracy is very high.
d) Digital circuits are less affected by noise.
e) Easy to perform error detection and execution with digital signal.
f) Integrated circuits are mostly used in the digital electronics, so that size of digital devices are small.

DISADVANTAGES OF DIGITAL ELECTRONICS:

i) Heat will be more when digital circuits are working more time.
ii) Digital circuits require a power supply.
iii) Digital circuits consume more energy or power as compare to any circuits.
iv) More complex circuits.
v) When one IC will be damaged it must affect to others.

APPLICATION OF DIGITAL ELECTRONICS:

i) Digital watch
ii) Refrigerator
iii) Speedometer
iv) Traffic light
v) Automatic glass door in offices and restaurant.
vi) Rocket science.
vii) ATM card
viii) Computer & laptops.

CONCLUSION:

We concluded that the above experiment has been done by me successfully.

Experiment - 2

AIM OF THE EXPERIMENT:

To study about NOT gate.

APPARATAUS REQUIRED:

i) Digital electronics kit
ii) Probes(connectors)
iii) Power supply

TRUTH TABLE:

INPUT	OUTPUT
A	$\overline{A}$
0	1
1	0

CONCLUSION:

We concluded that the above experiment has been done by me successfully.

Experiment - 3

AIM OF THE EXPERIMENT:-

To study about OR gate

APPARATUS REQUIRED:-

i. Digital trainer kit.
ii. Probes (connector)
iii. Power Supply.

TRUTH TABLE:-

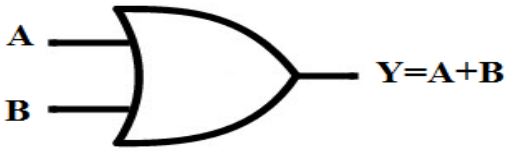
Input		Output
A	B	Q=A+B
0	0	0
0	1	1
1	0	1
1	1	1

.

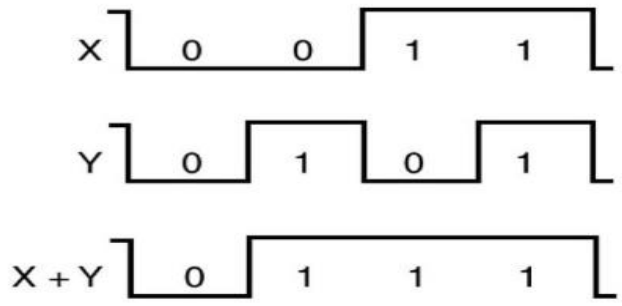
CONCLUSION:-

We concluded that the above experiment has been done successfully by us.

LOGIC GATE DIAGRAM:-



TIMING DIAGRAM:-



Experiment - 4

AIM OF THE EXPERIMENT:-

To study about AND gate.

APPARATUS REQUIRED:-

i. Digital trainer kit
ii. Probes(connectors)
iii. Power supply

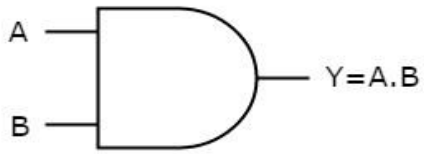
TRUTH TABLE:-

Input		Output
A	B	Q=A.B
0	0	0
0	1	0
1	0	0
1	1	1

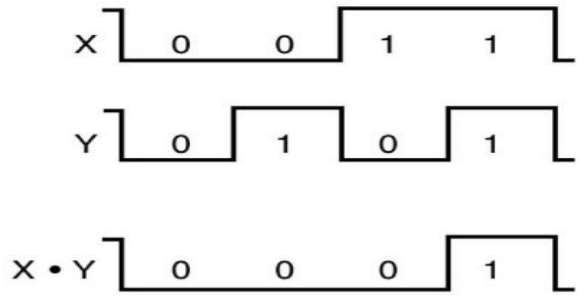
CONCLUSION:-

We concluded that the above experiment has been done by us successfully.

AND GATE DIAGRAM:-



TIMING DIAGRAM:-



Experiment - 5

AIM OF THE EXPERIMNT:-

To study about NAND logic gate

APPARATUS REQUIRED:-

i. Digital trainer kit
ii. Probes(connection)
iii. Power supply

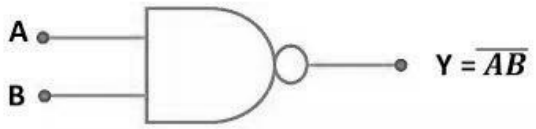
TRUTH TABLE:-

INPUT		OUTPUT
A	B	$Q=\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

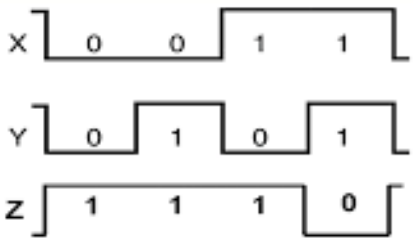
CONCLUSION:-

We concluded that the above experiment has been done by us successfully.

NAND gate diagram:-



Timing diagram:-



Experiment – 6

Aim of the experiment:-

To study about NOR logic gate

Apparatus Required:-

i)Digital trainer kit

ii) probes (connector)

iii) Power supply

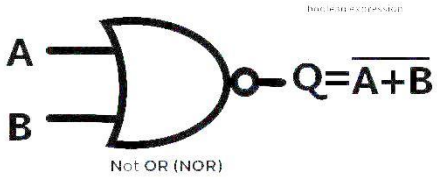
Truth Table:-

INPUT		OUTPUT
A	B	$Q=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

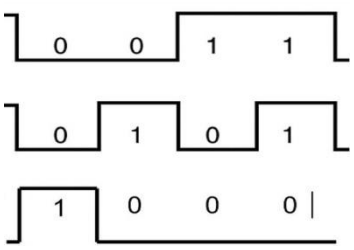
Conclusion:-

We conclude that the above experiment has been done by us successfully

Logic gate diagram:-



Timing diagram:-



Experiment – 8

Aim of the Experiment-

To study about x-nor gate

Apparatus Required:-

i)Digital trainer kit.

ii)probes(connector).

iii)power supply.

Truth Table:-

INPUT		OUTPUT
A	B	$Q=AB+\overline{A}\overline{B}$
0	0	1
0	1	0
1	0	0
1	1	1

Conclusion:-

We concluded that the above experiment has been done by us successfully.

Experiment – 9a

AIM OF THE EXPERIMENT:-

To implement various gates by using universal properties of NAND gates, verify and truth table tabulate data.

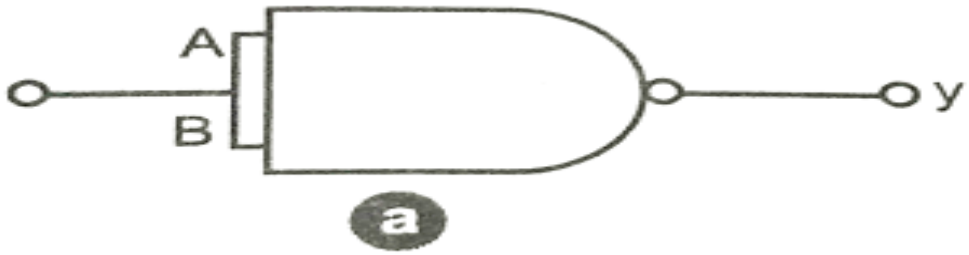
APPARATAUS REQUIRED:-

i) Digital electronic kit
ii) Probes(connector)
iii) Power supply

TRUTH TABLE:-

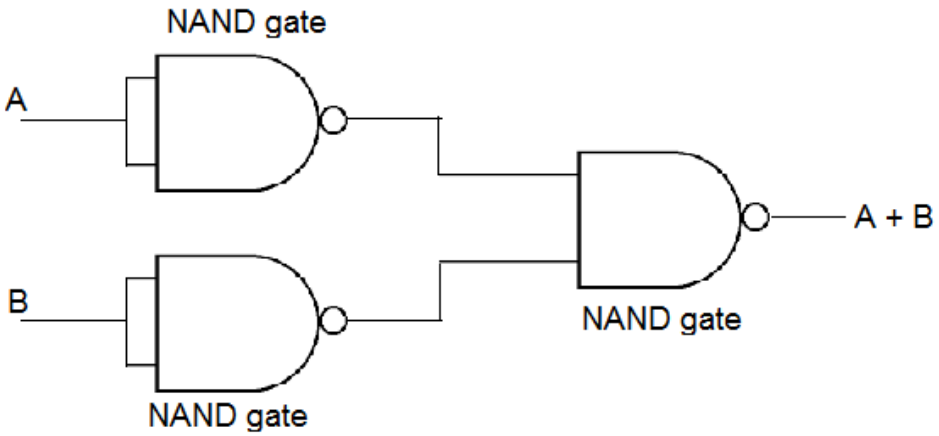
i) NOT gate using NAND gate

Input	Output
A	Y
0	1
1	0



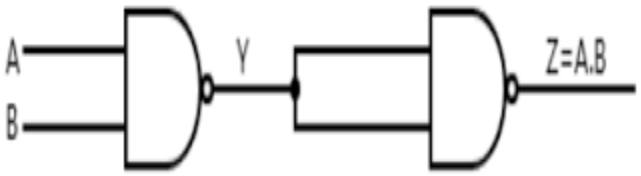
ii) OR gate using NAND gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



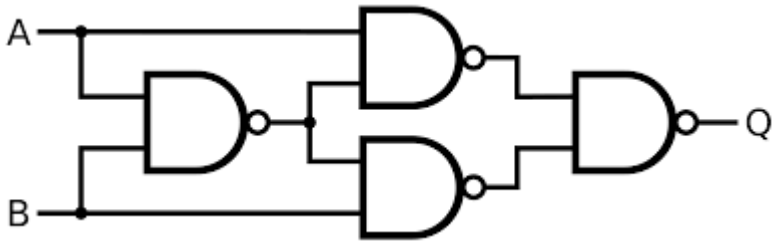
iii) AND gate using NAND gate

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



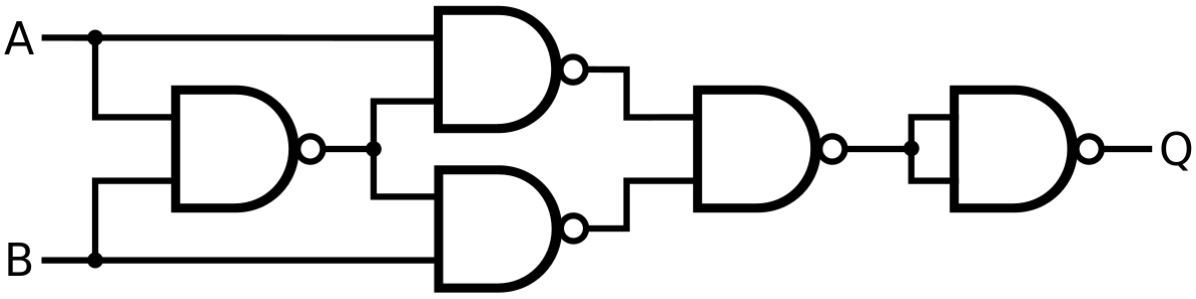
iv) X-OR gate using NAND gate

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0



v) X-NOR gate using NAND gate

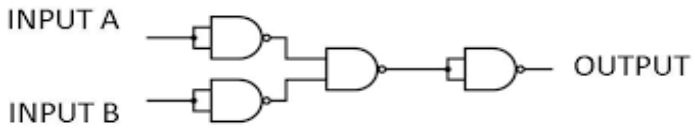
Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1



Experiment – 9b

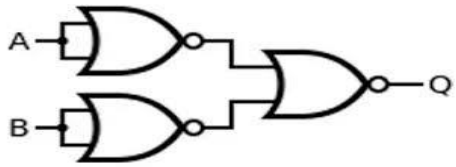
NOR gate using NAND gate:-

INPUT		OUTPUT
A	B	$Q=\overline{A.B}$
0	0	1
0	1	0
1	0	0
1	1	0



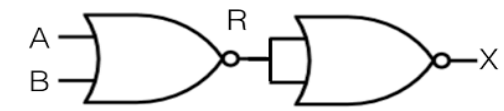
AND gate using NOR gate:-

Input		Output
A	B	Q=A.B
0	0	0
0	1	0
1	0	0
1	1	1



OR gate using NOR gate:-

Input		Output
A	B	Q=A+B
0	0	0
0	1	1
1	0	1
1	1	1



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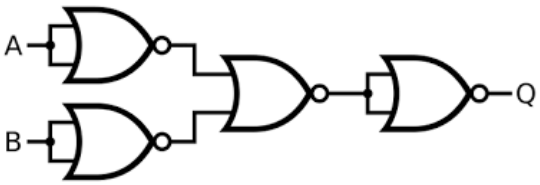
NOT gate using NOR gate:-

INPUT	OUTPUT
A	$\overline{A}$
0	1
1	0

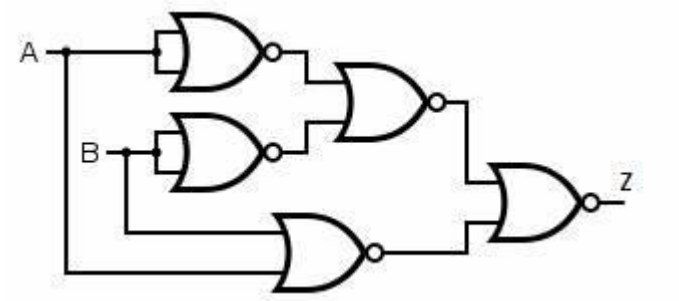
NAND gate using NOR gate:-

INPUT		OUTPUT
A	B	$Q=\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0



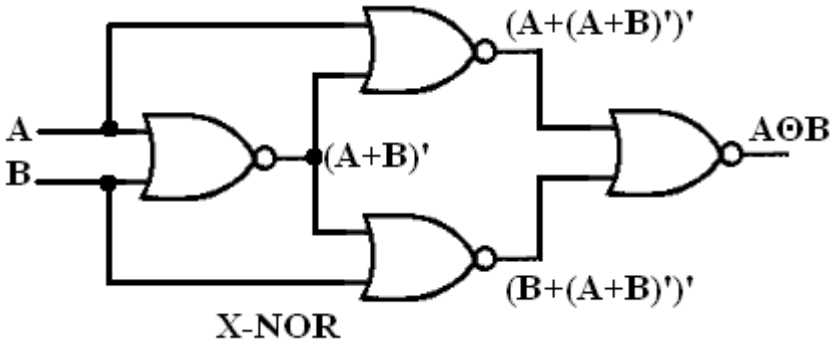
XOR gate using NOR gate:-

INPUTS		OUTPUTS
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



X-NOR gate using NOR gate:-

A	B	A **XNOR** B
0	0	1
0	1	0
1	0	0
1	1	1



Experiment – 10

AIM OF THE EXPERIMENT

To construct and verify operation of half adder & full adder using logic gates.

APPARATUS REQUIRED

i. Digital trainer Rit.
ii. Probes (Connector)
iii. Power supply.

TRUTH TABLE

Half adder

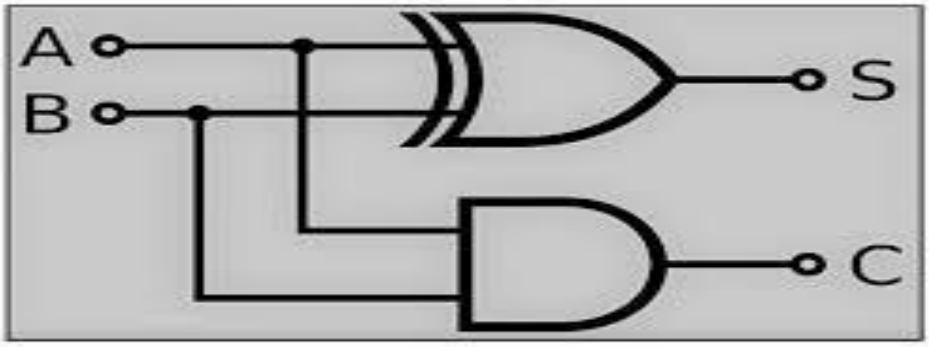
Input		Output	
A	B	Sum(s)	Carry(c)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder

Input			Output	
A	B	C	Sum(s)	Carry(c)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1

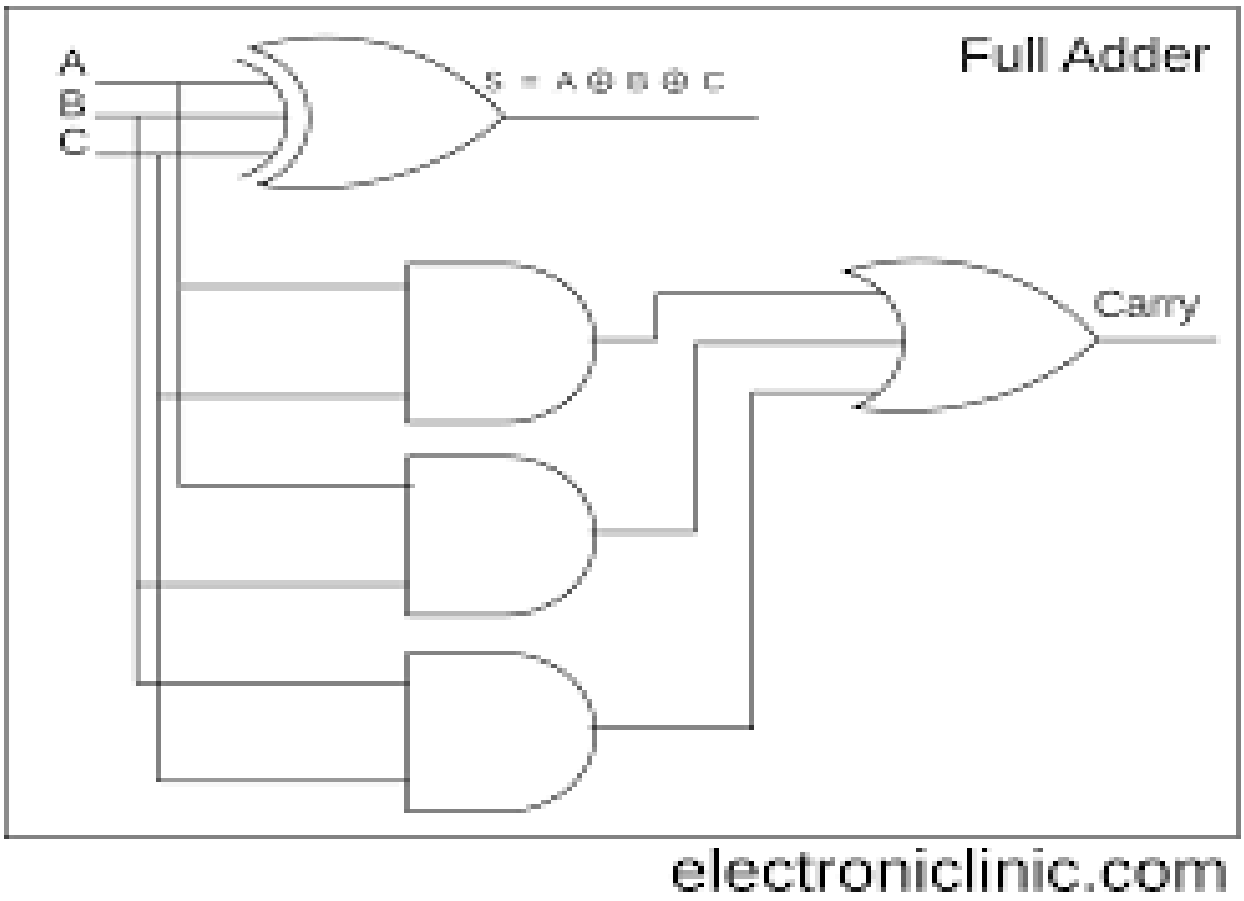
Intput			Output	
A	B	C	Sum(s)	Carry(c)
1	1	0	0	1
1	1	1	1	1

Logic gate diagram of half adder



HA Logical Diagram

Logic gate diagram of full adder



Conclusion

We concluded that the above experiment has been done by as successfully.

Experiment – 11

AIM OF THE EXPERIMENT:-

To design multiplexer (4:2) and Demultiplexer (1:4)

Apparatus required:-

a. Digital trainer kit
b. Probes (connector)
c. Power supply

Truth table:-

Multiplexer (4:1):

SELECTOR		OUTPUT
S_1	S_2	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Demultiplexer (1:4):-

Input selector output

S_1 S_0 D_0 D_1 D_2 D_3

Conclusion:-

We concluded that the above experiment has been done by us successfully.

Experiment – 12

AIM OF THE EXPERIMNT :-

To decide the operation of flip-flop

(i)S-r flip-flop (ii) j-k flip-flop (iii) d- flip-flop (iv) t- flip-flop

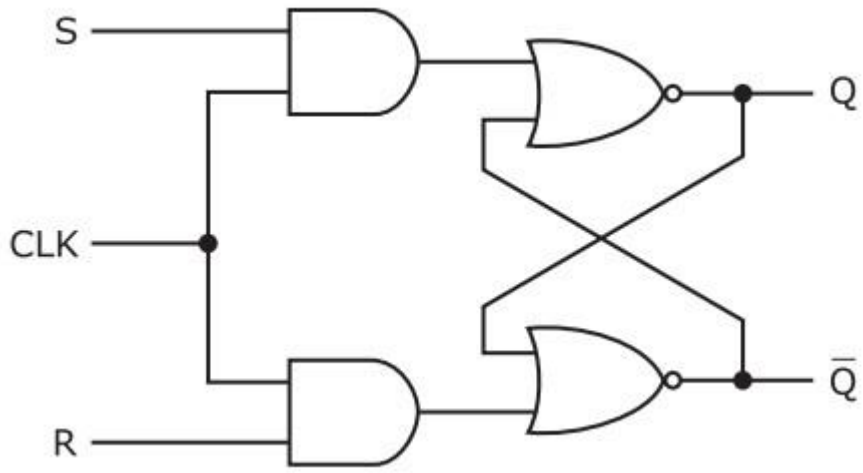
Apparatus required:-
(a)digital trainer kit
(b)probas (connector)
(c)power supply

Truth table:-
(i)SR flip flop:-

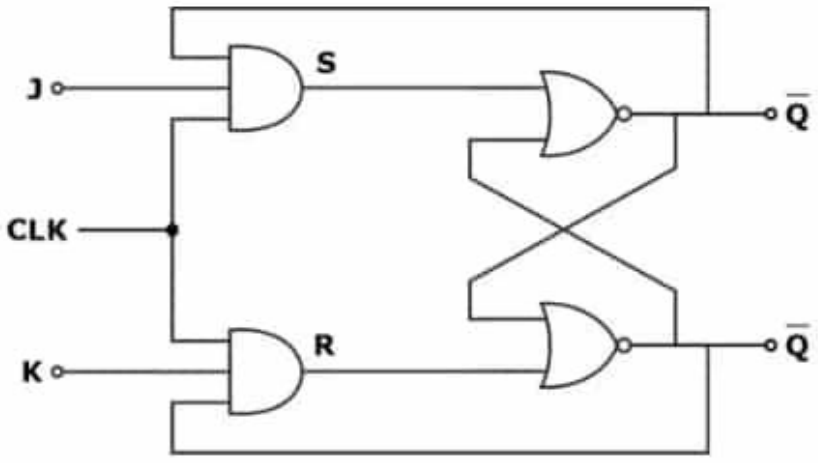
Input			output
Clk	S	R	Qn+1x
0	x	x	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	invalid

(ii)J.K flip flop:-

Input			Output
Clk	J	K	Q $\bar{Q}$
O	X	X	Memory state
1	0	0	Memory state
1	0	1	0 1
1	1	0	1 0
1	1	1	0 1



$\boxed{S = J\overline{Q}}$ and $\boxed{R = KQ}$



(iii) d- flip flop :-

Clk	D	Qn+1
0	x	Qn
1	0	0
1	1	1

(iv) t flip flop:-

Clk	T	Q	$\bar{Q}$
0	X	Memory state	
1	0	Memory	
1	1	Memory	

Conlusion:-

We concluded that the above experiment has been done by us succesfully.